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NEXGEN POWER SYSTEMS
VERTICAL GaN

CPES Power Management Consortium (PMC) Review Meeting

Robustness of Vertical GaN Fin-JFETs: Update on Avalanche and Short Circuit Tests

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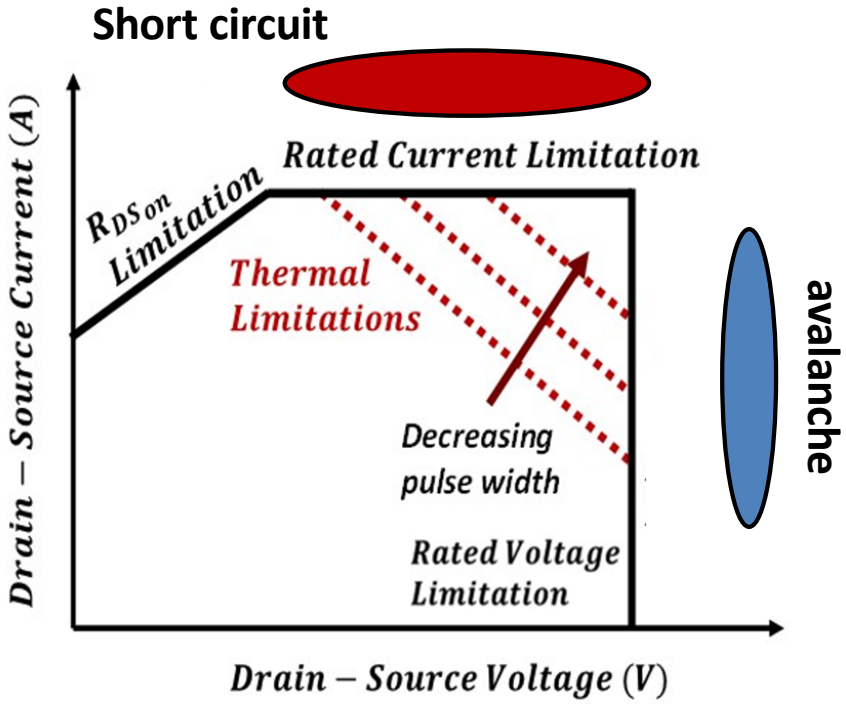
This is an excerpt of the full slides; for full slides, please contact Vikas Dhurka Vikas.Dhurka@nexgenpowersystems.com

Outline

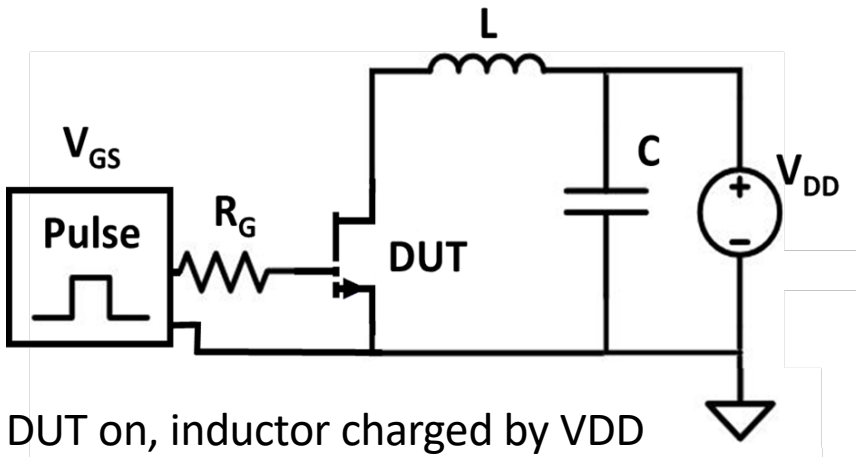
- Introduction
  - Robustness requirements: avalanche and short circuit
  - GaN fin-channel junction field-effect transistor (Fin-JFET)
- Avalanche test
  - Single-event test
  - Repetitive test
- Short circuit test
  - Single-event test
  - Benchmark
- Summary & next steps

Avalanche Robustness

Avalanche (surge-energy) and short circuit robustness are desired and required in power applications such as electric vehicle, motor drives, etc.



- Avalanche robustness is characterized by unclamped inductive switching (UIS) circuit

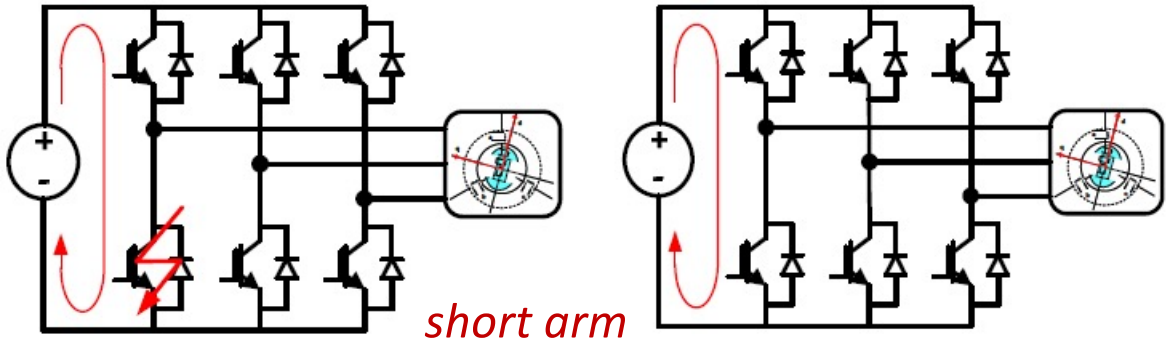


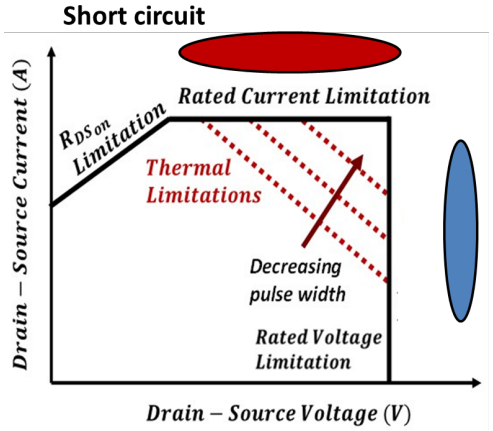
- DUT on, inductor charged by VDD
- Inductor current reaches desired value, DUT off
- Energy stored in L goes through off-state DUT

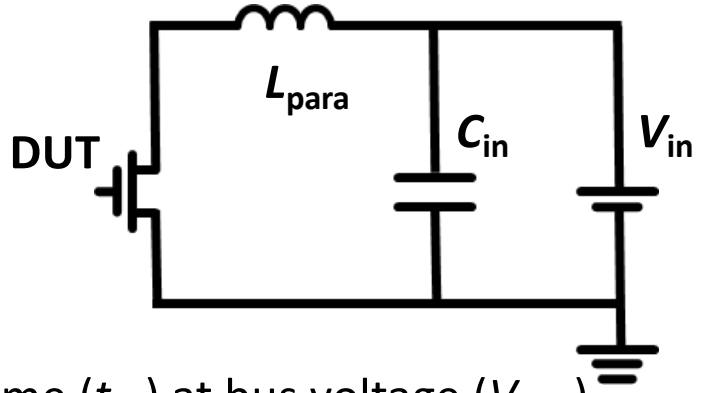
- Power MOSFETs: dissipate energy via avalanche process, E_{AVA} acts as critical parameter

Short Circuit Robustness

- Different types of Short Circuit event in application
  - Hard switching fault (HSF, SC type I): $V_{DS} = V_{BUS}$
  - Fault under load (FUL): device ON, V_{DS} low
  - Type III: 3rd-quad, reverse ON
- HSF is most harsh, and most commonly used.





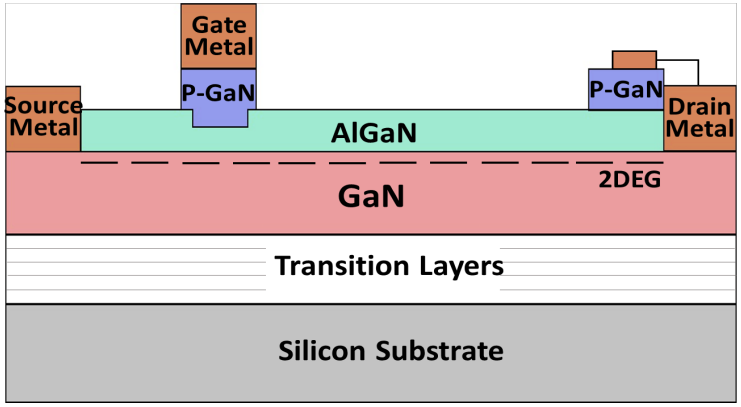


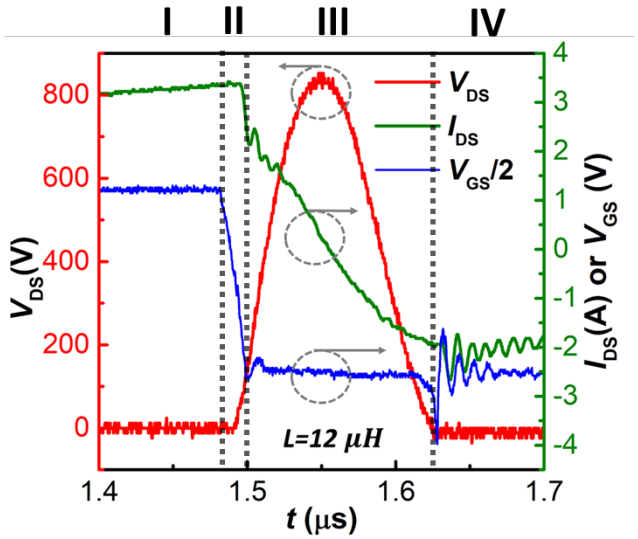
- General requirement: 10 µs short circuit withstanding time (t_{SC}) at bus voltage (V_{BUS})

Z. Xu and F. Wang, "Experimental investigation of Si IGBT short circuit capability at 200°C," 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2012, pp. 162-168

Challenge of GaN HEMT: Lack of Avalanche Capability

- No p-n junction connected to electrodes: no avalanche mechanism



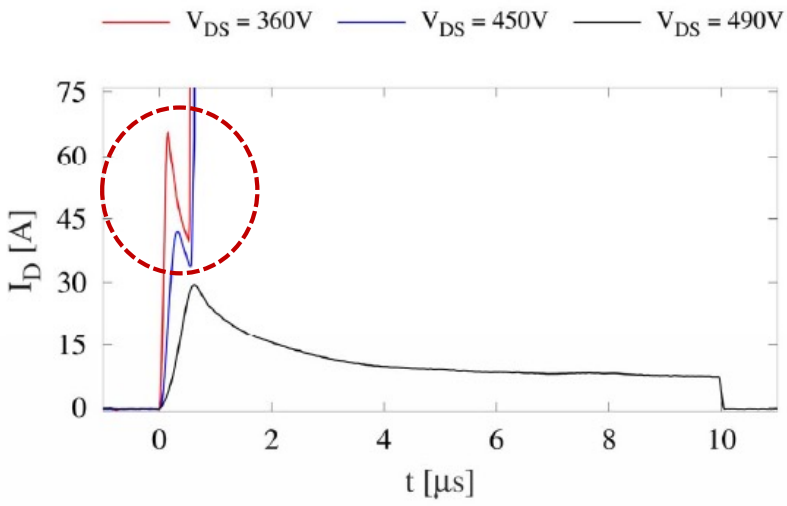


- GaN HEMTs transfer the energy through capacitive charging
  - Failure determined by transient breakdown voltage
  - Can withstand surge-energy in tens of μJ, much smaller than MOSFETs (in mJ)

R. Zhang, J. P. Kozak, M. Xiao, J. Liu and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," in IEEE Transactions on Power Electronics, vol. 35, no. 12, pp. 13409-13419, Dec. 2020

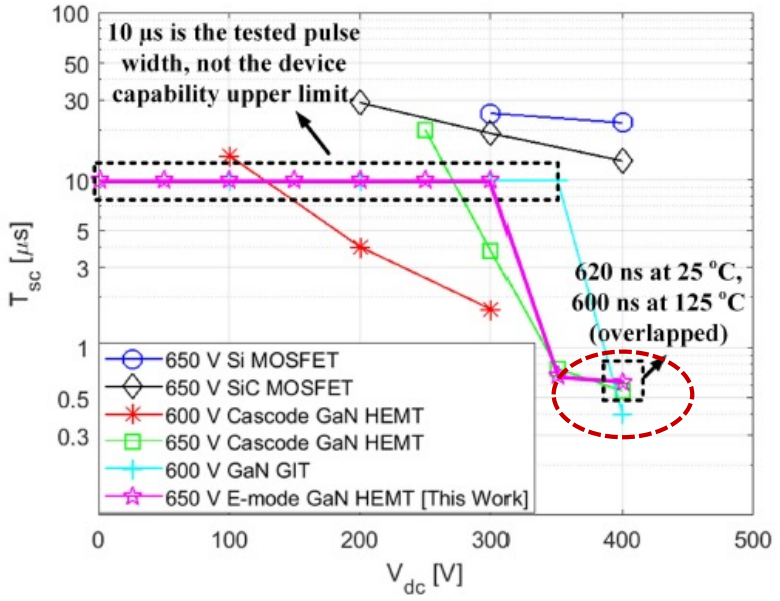
Challenge of GaN HEMT: Low Short Circuit Robustness

Reported t_{SC} of all types of commercial 650 V GaN HEMTs is below 1 µs at 400 V V_{BUS}



(*490 V test was done by larger R_G and higher L*)

A. Castellazzi, A. Fayyaz, S. Zhu, T. Oeder and M. Pfost, "Single pulse short-circuit robustness and repetitive stress aging of GaN GITs," 2018 IEEE International Reliability Physics Symposium (IRPS), 2018, pp. 4E.1-1-4E.1-10

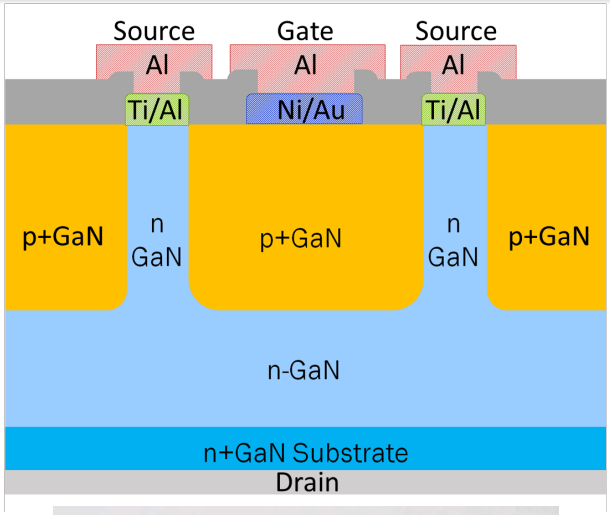


H. Li et al., "Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions," in IEEE Transactions on Industry Applications, vol. 55, no. 2, pp. 1807-1816, March-April 2019

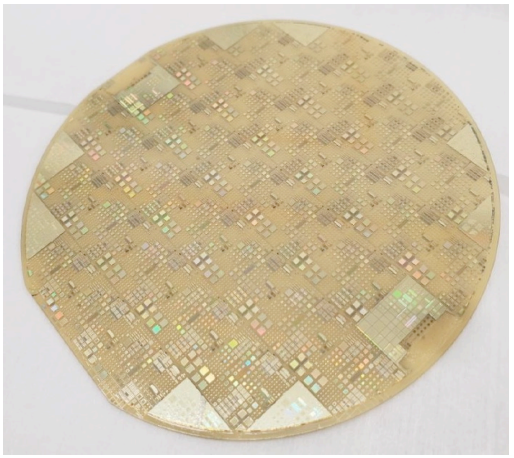
The short circuit robustness concern becomes a major roadblock for GaN penetrating in EV powertrains

GaN Fin-JEFT Fabrication

- NexGen's normally off Vertical JFET design
- 1 µm deep nGaN fin (source)
- Gate on pGaN (gate)
- Ohmic back contact (drain)
- 650-700 V rated
- 0.1 mm^2 active region



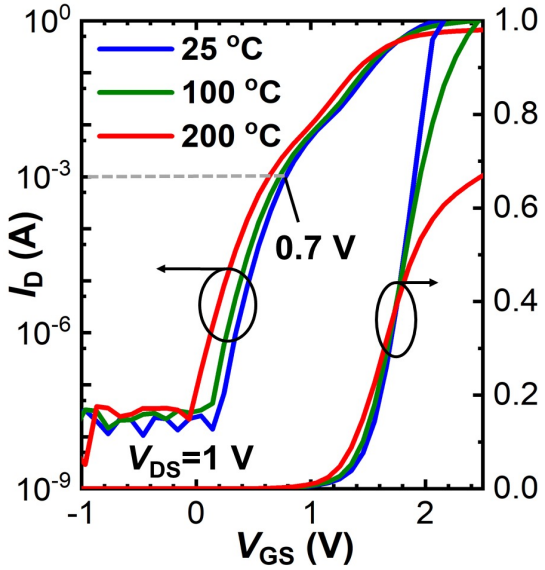
- Epi & fab processing in NexGen's facility (NY)
- 4" bulk Si doped n^+GaN substrates
- TO-247-4L package



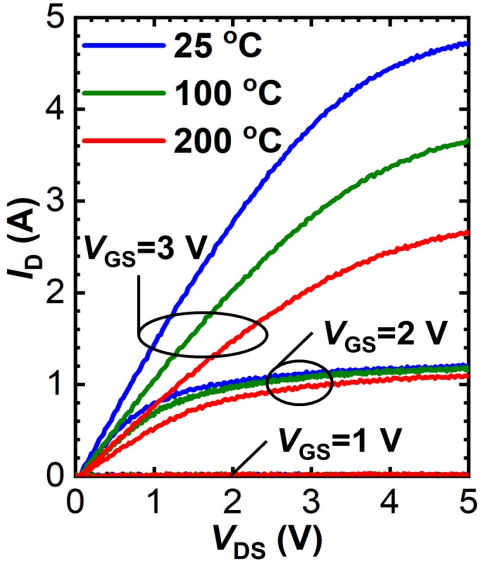
J. Liu et al., "1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability," in IEEE Transactions on Electron Devices, vol. 68, no. 4, pp. 2025-2032, April 2021

J. Liu et al., "1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities," 2020 IEEE International Electron Devices Meeting (IEDM), 2020, pp. 23.2.1-23.2.4

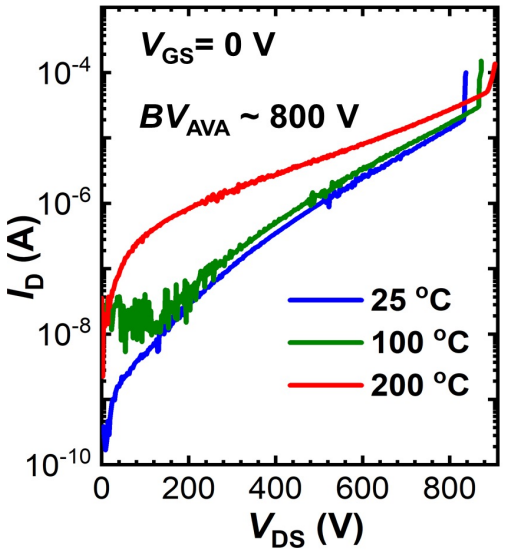
GaN Fin-JEFT Characterization



E-mode operation,
0.7 V V_{th}



~ 5 A saturation
current



Non destructive
avalanche ~ 800 V

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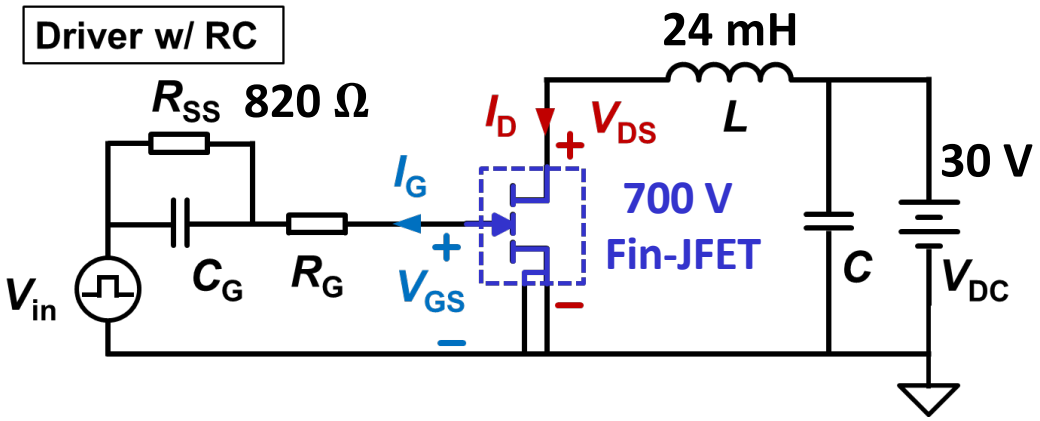
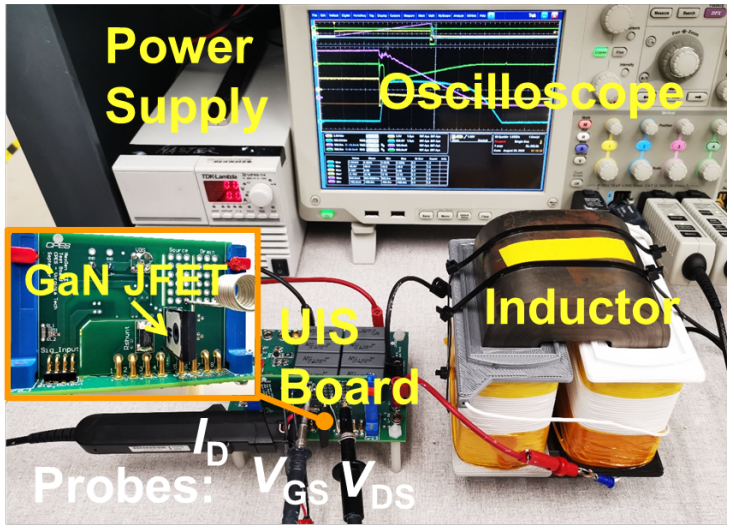
Avalanche Test Setup

UIS circuit used for the avalanche test

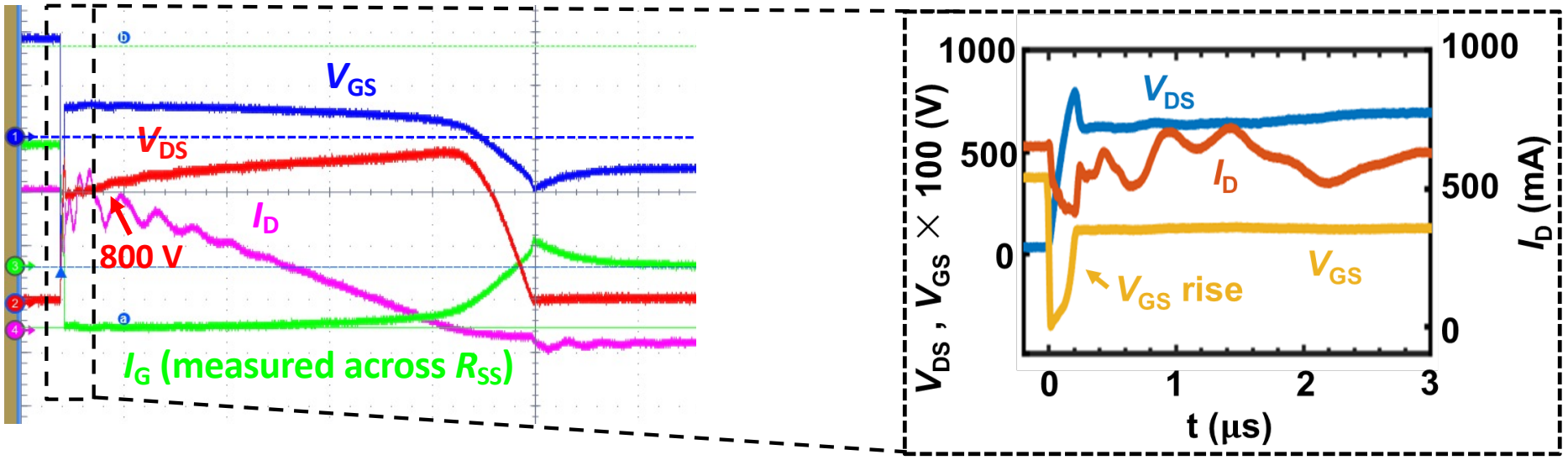




P-N junction at gate, RC gate driving circuit used

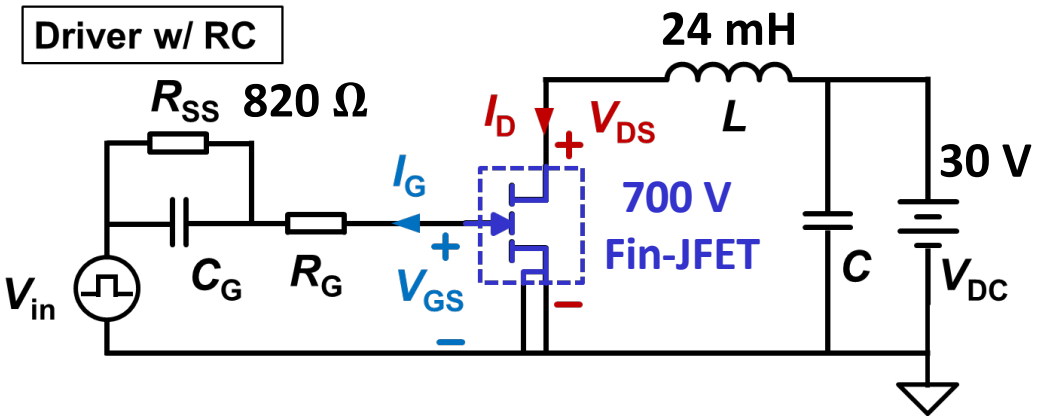
- Enables fast switching
- Suppress quiescent gate current

Typical Avalanche Test Waveforms



- Avalanche breakdown with a positive temperature coefficient
- Energy dissipated via internal avalanche
- V_{GS} was lift when entering avalanche breakdown

Repetitive Avalanche Test Setup



Avalanche through the Fin channel

3 s interval

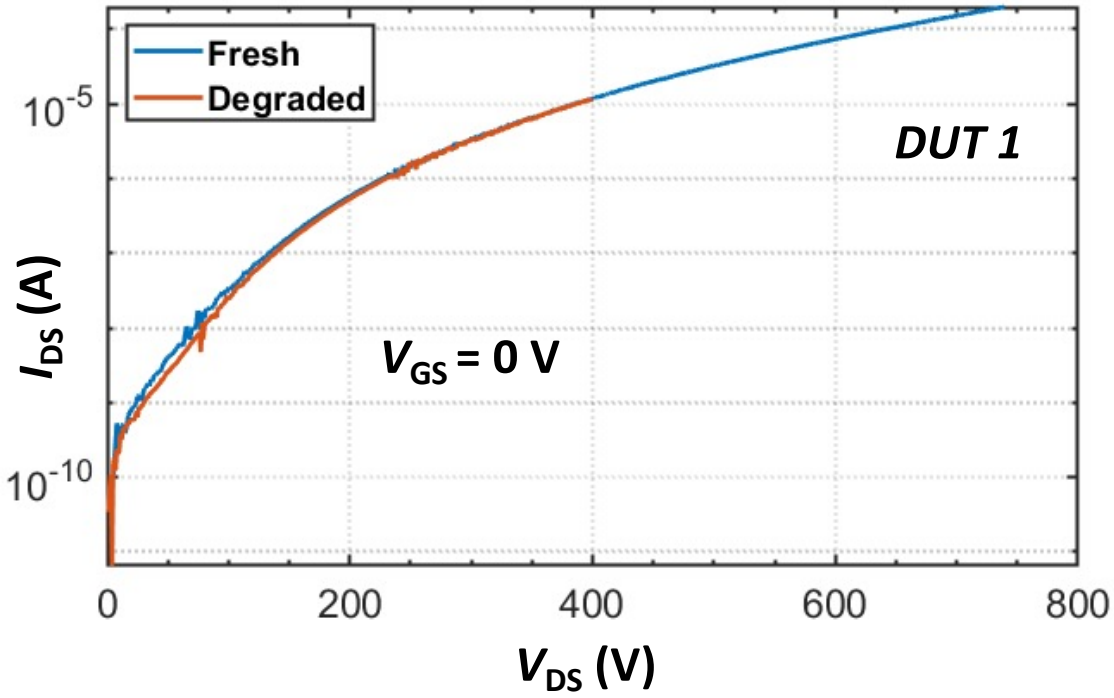
~ 7 mJ E_{AVA} each cycle (70% critical E_{AVA}), no temperature build up

All waveforms are recorded during the test

Failure Analysis: Final Failure

Device measured after completely failure (cyc #3705)

GS are short, only I_{DSS} was characterized



I_{DSS} shows almost no change
Suggesting the failure
between Gate and Source
"Failed open"

GaN Fin-JFET Avalanche Robustness Benchmark

V_{GS} (V)	Max Breakdown Voltage (V)		Dissipated Energy (mJ)	
	T = 25 °C	T = 100 °C	T = 25 °C	T = 100 °C
−10	404	401	548	542
−12	562	568	569	570
−14	729	750	595	593
−16	925	942	607	600
−18	1076	1134	606	589
−20	1244	1275	585	621

Parameters	SiC JFET	NexGen GaN FinFET
Avalanche Voltage (V)	1200	800
Active Area (mm^2)	7	0.1
Testing condition	25 s, repetitive	3 s, repetitive
Critical E_{AVA} (mJ)	621	7~10
Normalized E_{AVA} (mJ/mm^2)	88.7	100.0

B. N. Pushpakaran et al., "High Temperature Unclamped Inductive Switching Mode Evaluation of SiC JFET," in IEEE Electron Device Letters, vol. 34, no. 4, pp. 526-528, April 2013

GaN Fin-JFET shows comparable E_{AVA} to the reported SiC JFET

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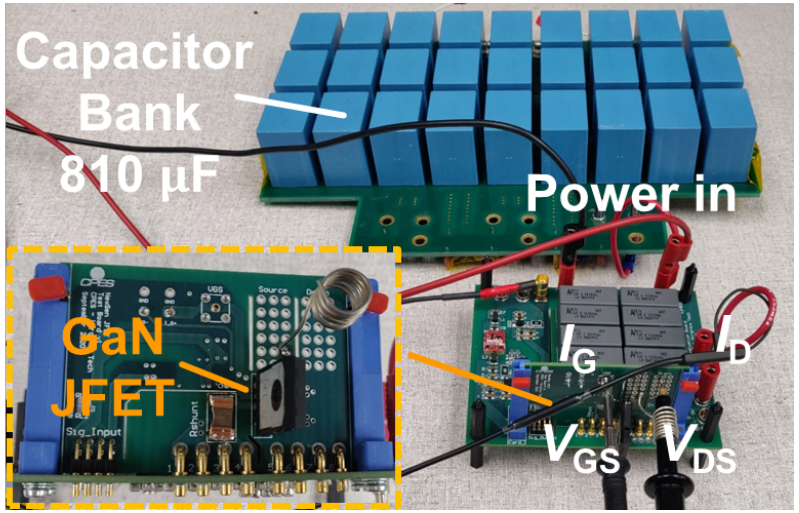
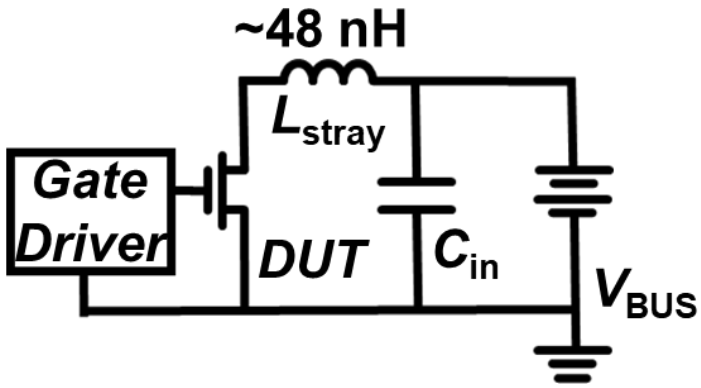
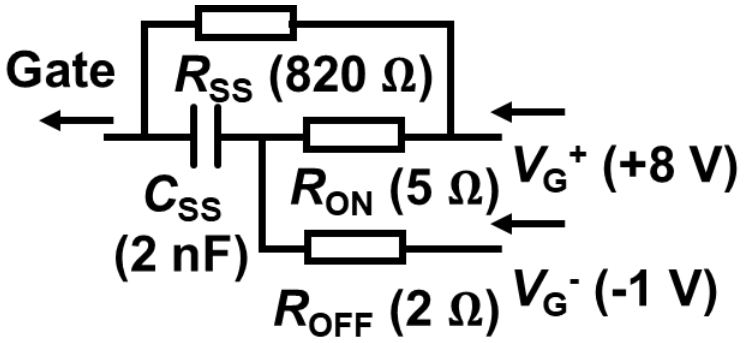
Short Circuit Test Setup

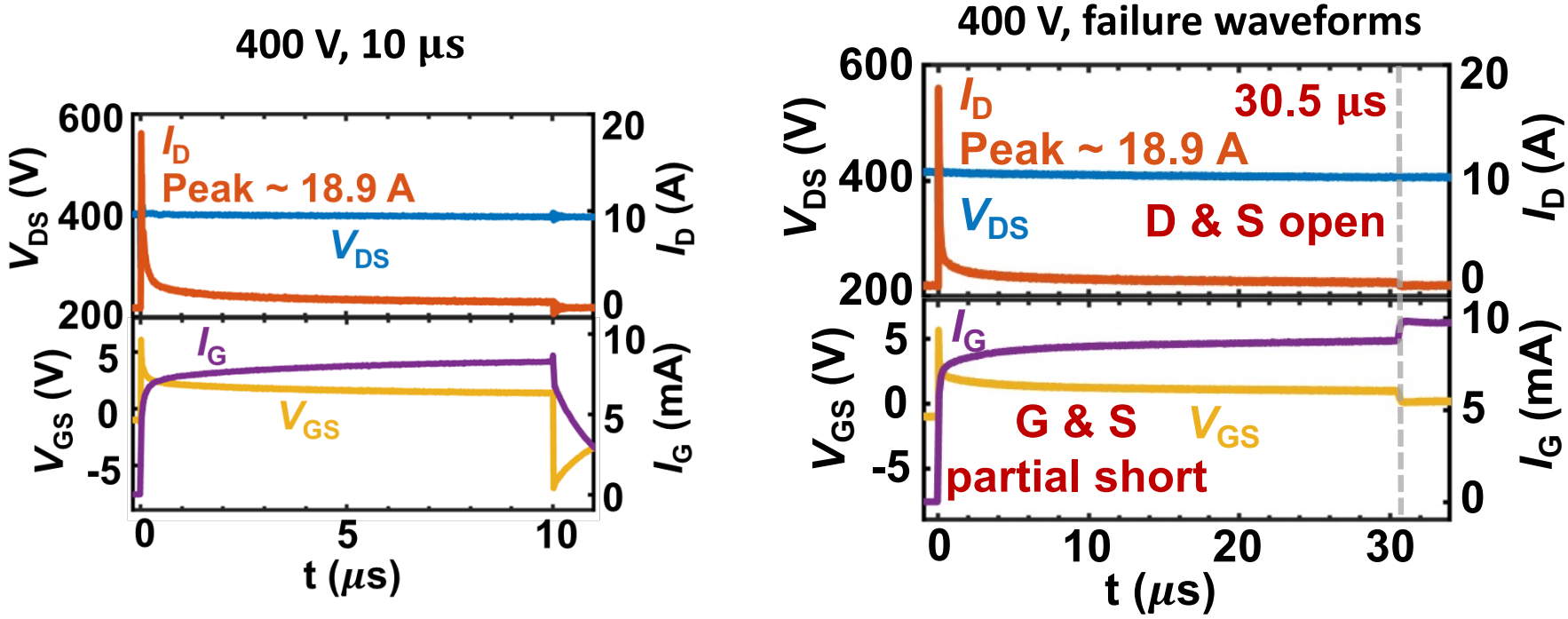






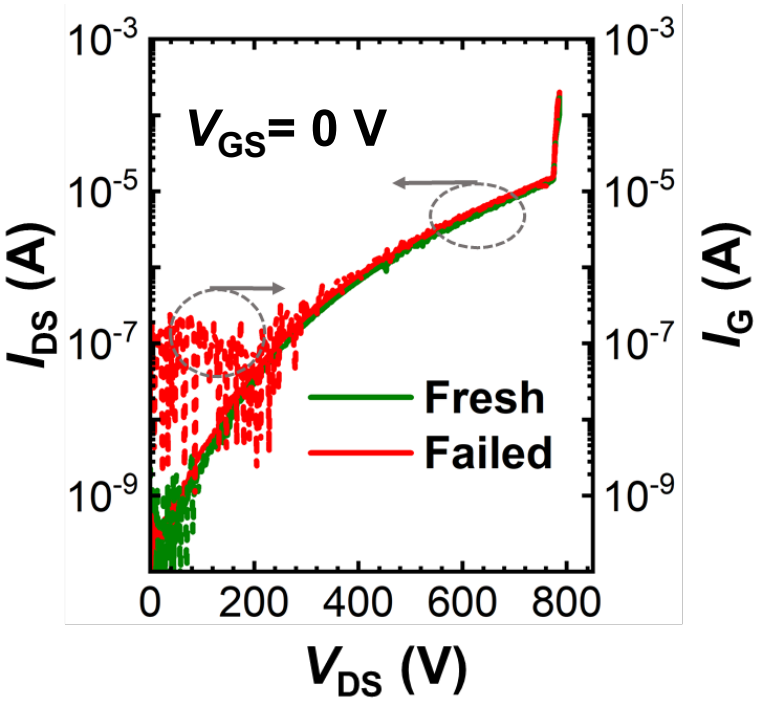
- Identical driving circuit to switching application
- No load inductor (~ 48 nH PCB parasitic)
- External capacitor bank (810 µF) for stable voltage
- V_{GS}, V_{DS}, I_{DS}, I_G (across R_{SS}) were measured

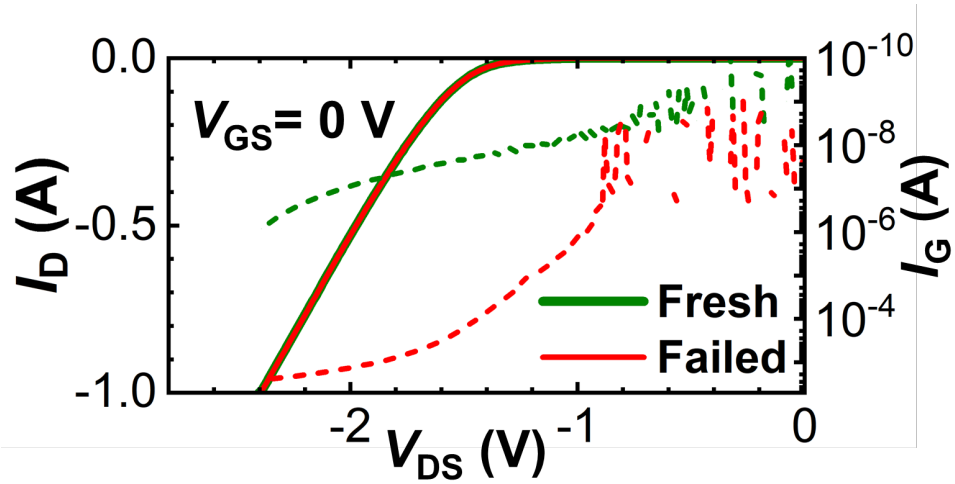
Safe Withstanding and Failure Waveforms



- A rapid increase in I_D, reaches peak in ~ 20 ns
- A decrease in V_{GS} due to the rise in I_G increases the voltage drop across R_{SS}
- DUT fails in 30.5 µs at 400 V V_{BUS}
- No change in V_{DS}, V_{GS} drops to 0, indicating a D-S open & G-S short failure nature

Failure Characterization & TCAD Simulation





- After failure, the DUT retains avalanche capability
- No change in reverse conduction current, while an increase in gate leakage observed
- Failure solely located between gate and source

GaN Fin-JFET Short Circuit Robustness Benchmark

Device	Type & reference	Volt. Rate (V)	Specific Ron (mΩ·cm2)	V_{bus} (V)	t_{SC} (µs)	E_{SC} a) (J/cm²)	Fail
Vertical GaN Fin-JFET (This work)		**700**	**0.7**	**400**	**30.5**	**7.5**	**open**
GaN HEMTs (p-gate, GIT, cascode)	Comm. [1]	600-650	N/A	400	0.62	N/A	short
	R&D [2]	650	N/A[d)]	400	3	N/A	N/A
	R&D [3]	650	19 Ω·mm[f)]	400	4-10	N/A	N/A
SiC/Si JFET cascode [4]		650	1.05	400	10	N/A	N/A
SiC MOSFET	Comm. [5]	650	N/A	400	13	N/A	open
	R&D [6]	650	7.2	400	8.4	6.0	N/A
Si CoolMOS	Comm. [6]	650	10	400	19	6.7	N/A

[1] H. Li et al., IEEE Trans. Ind. Appl., vol. 55, no. 2, pp. 1807, Mar. 2019.
[2] D. Bisi et al., in 2021 IEEE APEC, pp. 370, Jun. 2021
[3] I. Hwang et al., IEEE Electron Device Lett., early access online, 2021.
[4] A. Bhalla et al., in 2019 ISPSD, pp. 191, May. 2019.
[5] N. Badawi et al., in IEEE ECCE, Sept. 2016.
[6] A. Agarwal et al., IEEE Trans. Power Electron., vol. 36, no. 3, pp. 3335, Mar. 2021.

- GaN Fin-JFET shows the longest t_{sc} among 600-700 V rated unipolar transistors
- The failure-to-open nature is highly desirable in applications

Summary

- **Summary**
  - **A unique "avalanche through fin-channel" phenomena was identified in GaN Fin-JFET**
  - **The E_{AVA} of GaN Fin-JFET is comparable to SiC devices.**
  - **Under 70% of critical , GaN Fin-JFET survived over 1k cycles of repetitive avalanche test**
  - **GaN Fin-JFETs show failure-to-open nature in both repetitive avalanche test and single-event short circuit test, which is highly desirable for system applications.**
  - **GaN Fin-JFET shows great avalanche & short circuit robustness.**

Thank you!

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