Avalanche Ruggedness of 600/650 V Lateral GaN HEMTs and 1200 V Vertical GaN Diodes

Ruizhe Zhang, Jingcun Liu, Joseph Kozak, Yuhao Zhang

Email: {rzzhang, jcliu, yhzhang}@vt.edu

Outline

- Introduction
  - Avalanche test: Unclamped Inductive Switching (UIS) test
  - Open question: Avalanche capability in GaN-based power devices
- Avalanche test of 600/650 V lateral HEMTs
  - UIS tests under different temperatures
  - Failure analysis
- Avalanche test of 1200 V vertical GaN PN diode
  - Device static characterization
  - UIS tests under different temperatures
- Summary & Future Work

Outline

- Introduction
  - Avalanche test: Unclamped Inductive Switching (UIS) test
  - Open question: Avalanche capability in GaN-based power devices

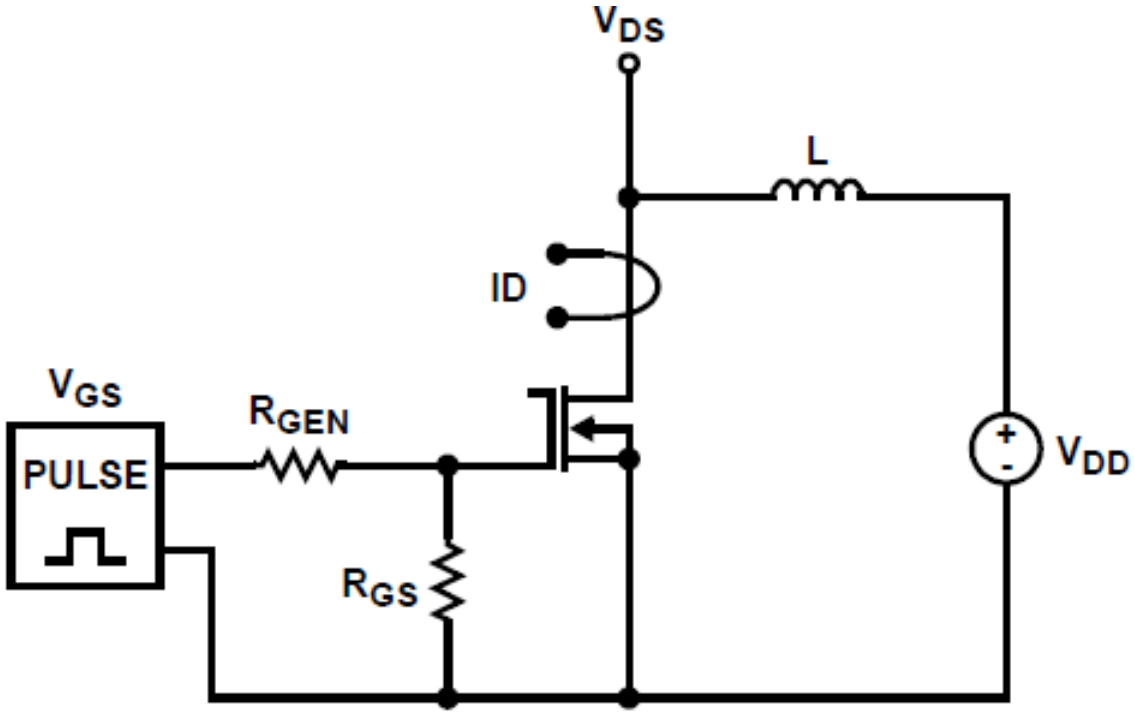
- Avalanche test of 600/650 V lateral HEMTs
  - UIS tests under different temperatures
  - Failure analysis

- Avalanche test of 1200 V vertical GaN PN diode
  - Device static characterization
  - UIS tests under different temperatures

- Summary & Future Work

Unclamped Inductive Switching (UIS): Avalanche Test

- Device surge-energy ruggedness is desired in many power applications : electric vehicle, motor drives, etc.
- Surge-energy capability typically characterized by unclamped inductive switching (UIS) test.



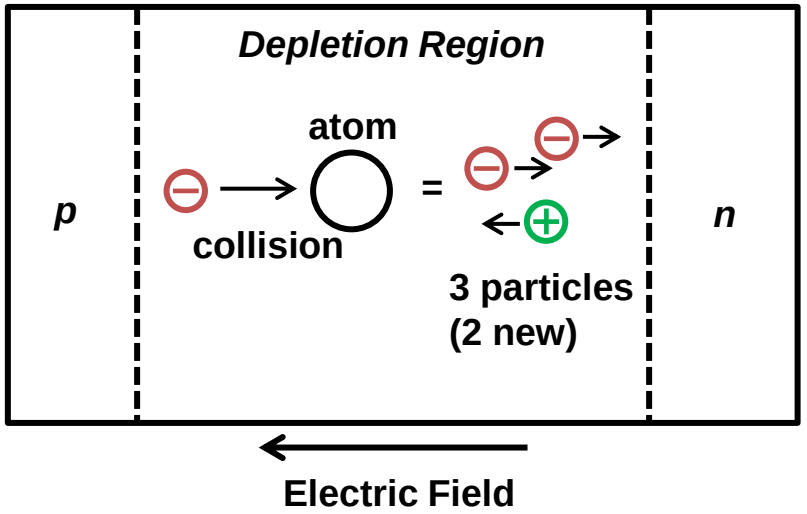
- DUT on, inductor charged by VDD
- Inductor current reaches desired value, DUT off
- Energy stores in L goes through off-state DUT

Si / SiC power MOSFETs:
Surge energy is dissipated by avalanching in DUT

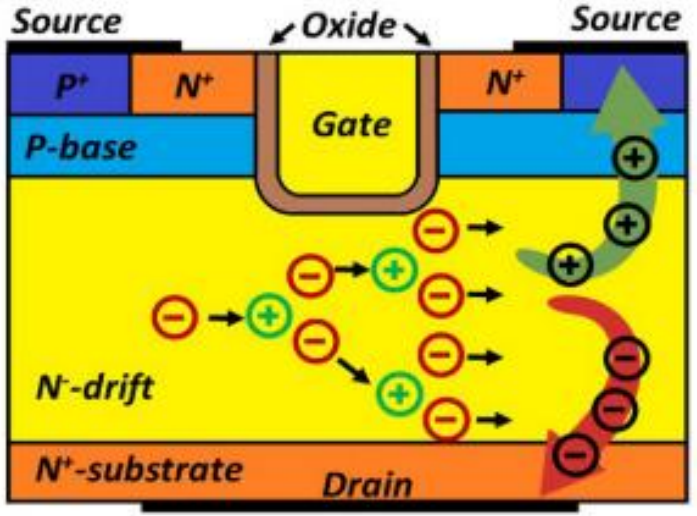
The Avalanche Phenomenon

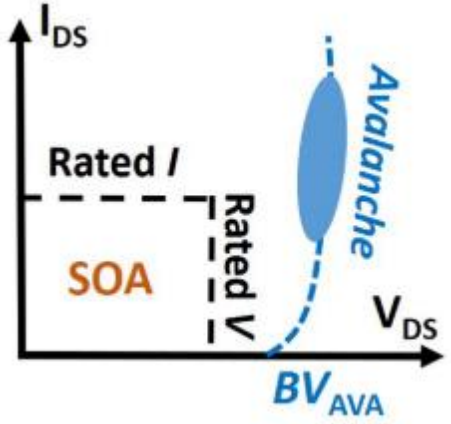
- **Impact ionization + positive feedback**

Multiplied electron-hole pairs at junction



Si/SiC MOSFET





- **Built-in safety mechanism**

Accommodate high current at BV_{AVA}

Recoverable within certain energy

E_{AVA}: Key metric for robustness

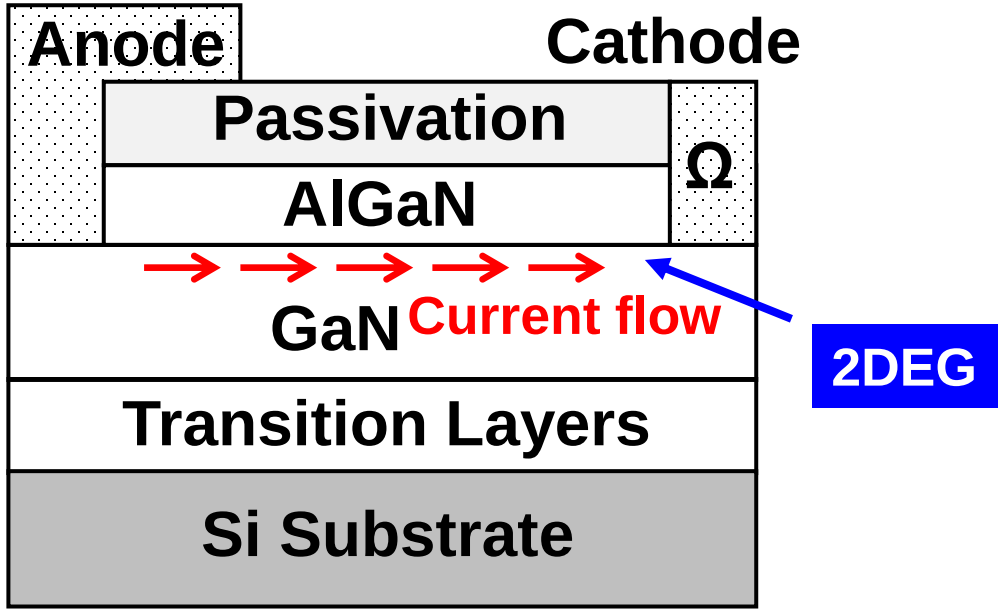
Key to avalanche:

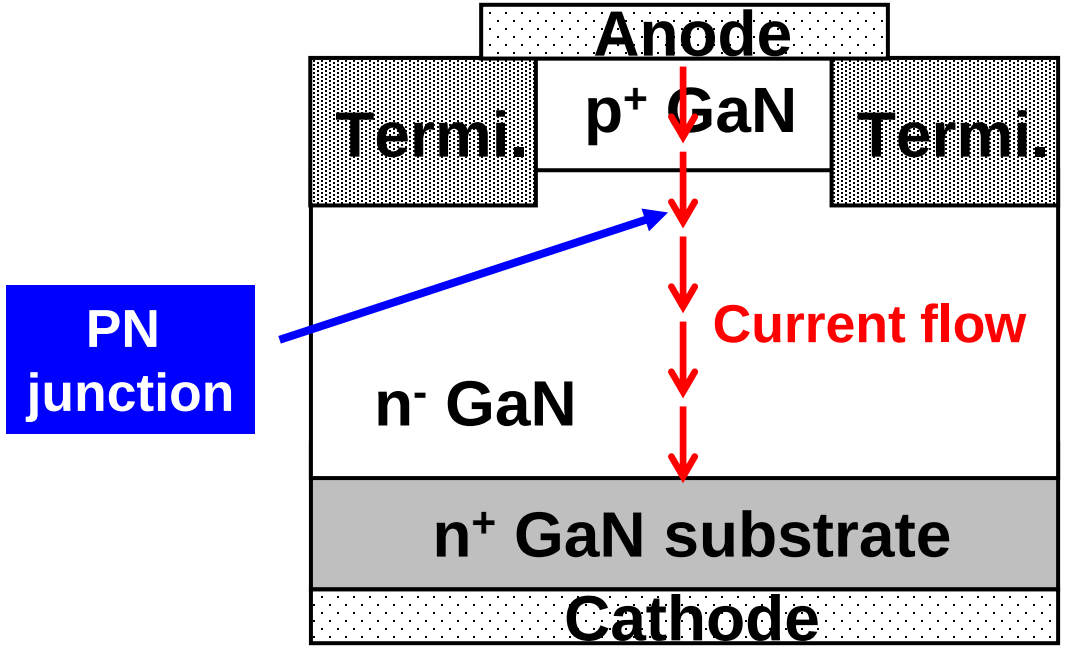
PN junction connected to electrodes

- **Breakdown voltage increases with temperature**

(Evidence for avalanche mechanism in practice for GaN & 4H-SiC)

Lateral GaN v.s. Vertical GaN





- 2DEG: Induced by piezoelectric effect: no doping
- No PN junction connected to electrodes
- Commercialized from 15 V to 650 V (-> 900 V)

- No PN junction connected to electrodes
- Currently under extensive study for potential medium-voltage, robust power applications

Open Questions

- How does GaN HEMT withstand/dissipate surge energy?
- What determines the withstand capability?
- What is the failure/degradation mechanism?

- Is there robust avalanche in GaN vertical PN diode?
- Is the avalanche energy comparable to Si / SiC MOSFETs?

Outline

- Introduction
  - Avalanche test: Unclamped Inductive Switching (UIS) test
  - Open question: Avalanche capability in GaN-based power devices

- Avalanche test of 600/650 V lateral HEMTs
  - UIS tests under different temperatures
  - Failure analysis

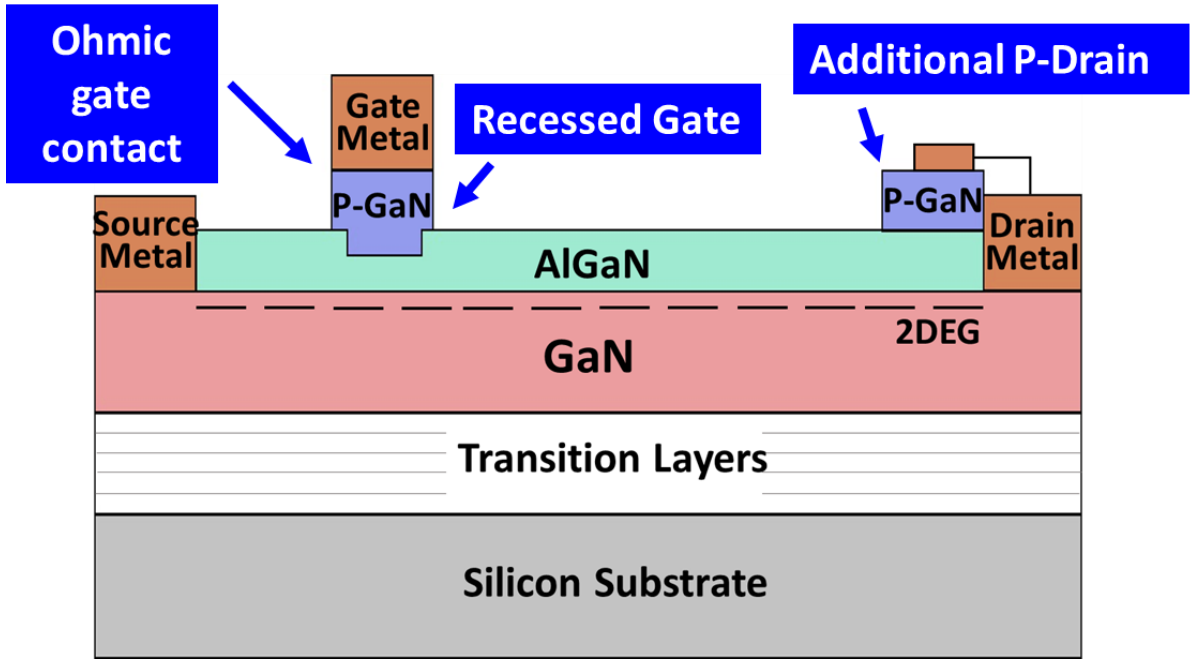
- Avalanche test of 1200 V vertical GaN PN diode
  - Device static characterization
  - UIS tests under different temperatures

- Summary & Future Work

Single-event UIS Test: DUTs

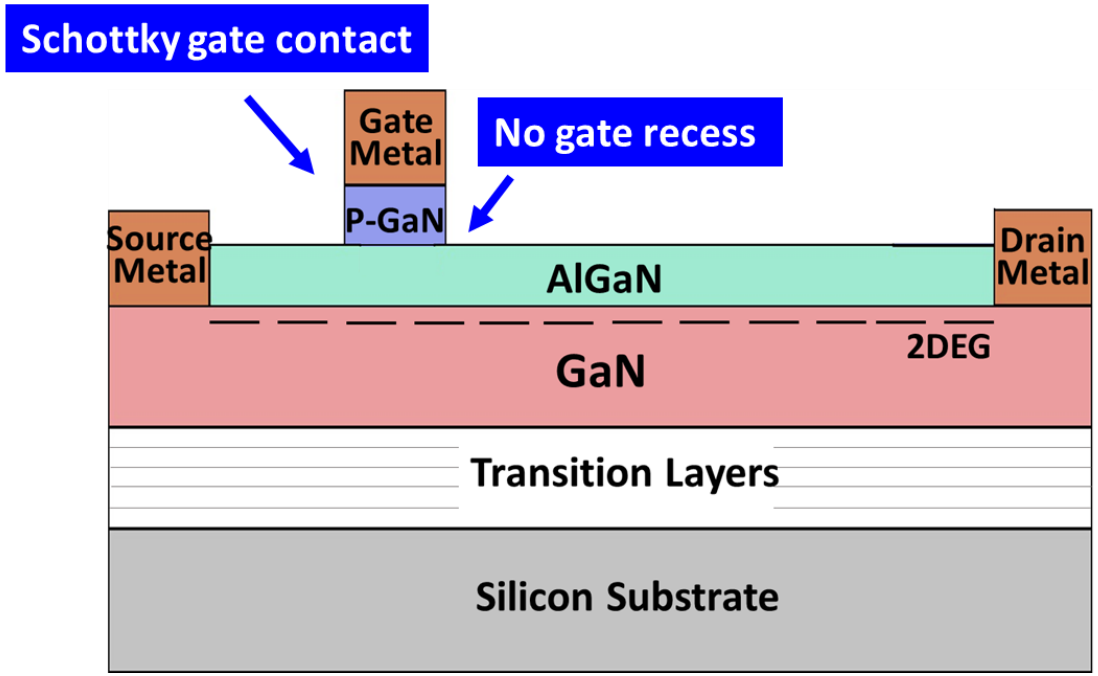
Company A: Gate Injection Transistor (GIT)
Device rating: 600 V, 31 A

V_{GS}(on) is clamped at 3.0~3.4 V
(same as GaN PN diode V_F)



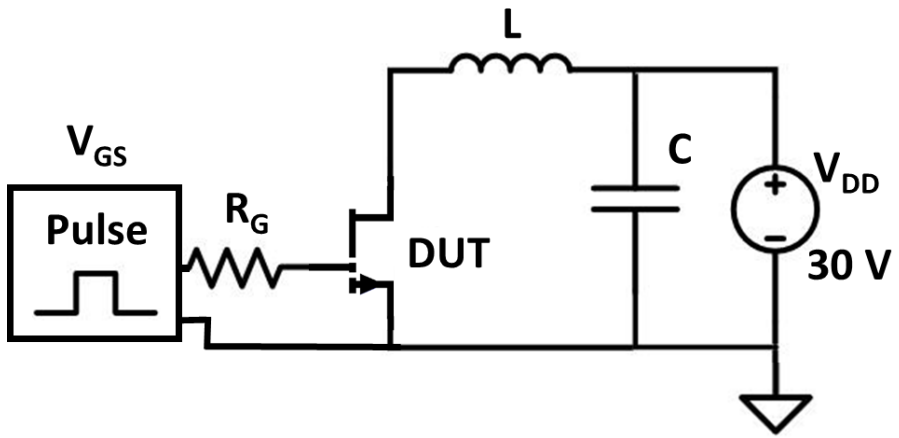
Company B: Schottky p-gate HEMT (SP-HEMT)
Device Rating: 650 V, 30 A.

V_{GS}(on) can safely go up to 7 V



Temperature Adjustable UIS Test Setup

Presented in PMC review, Dec. 2019



Mother Board: Power loops

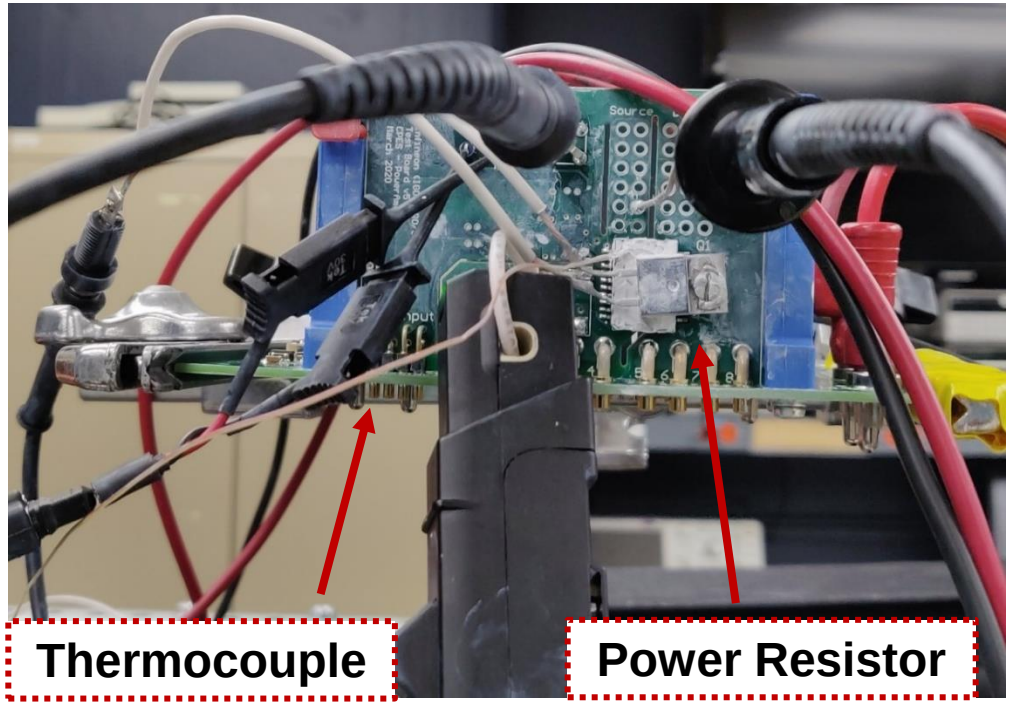
Daughter Card: Gate Driving Loop + DUT

V_{DD}=30 V

$V_{GS(ON)}$= 5 V (clamped to 3.0~3.4 V on GIT)

$V_{GS(OFF)}$ = -5 V

New board & setup enabling high-T tests

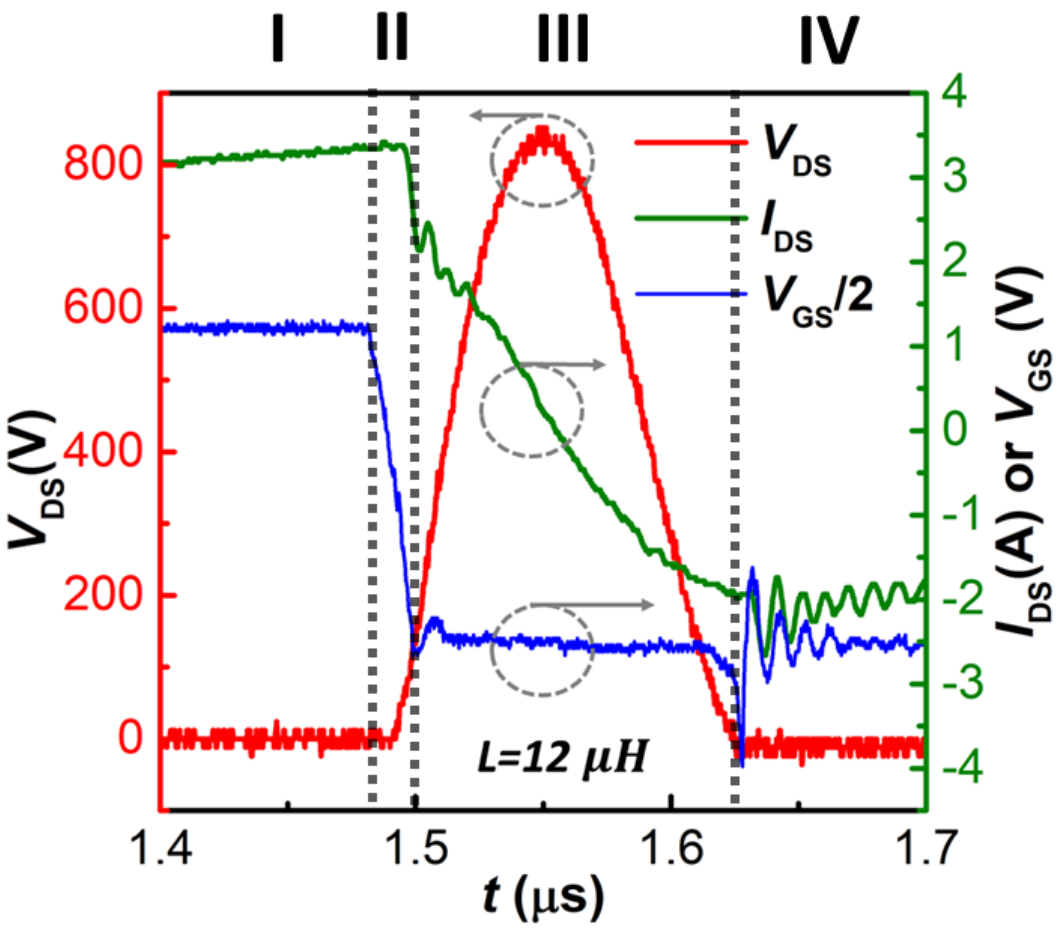


A TO-220 power resistor was used to heat up the DUT

High temperature FR-4 was used for the PCB

UIS Test Result – Safe Withstanding

Withstanding process:



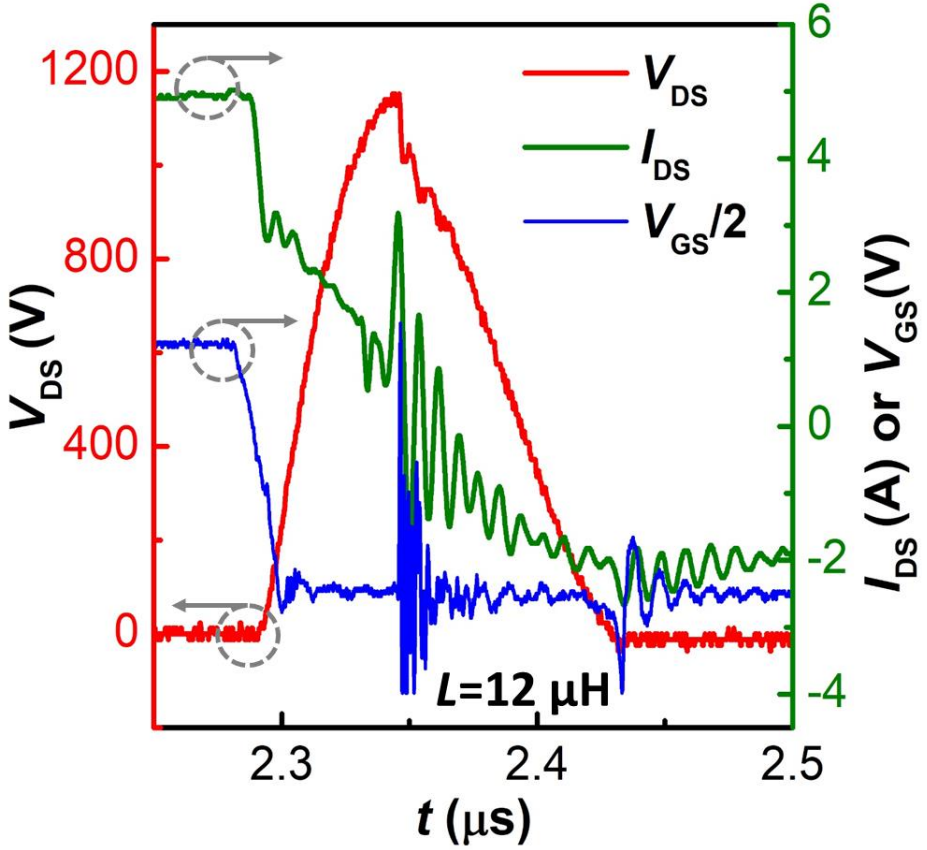
- **I: Device on, inductor charging.**
- **II: Device turn-off.**
- **III: Resonance between inductor & device C_{oss}, little energy dissipation in this stage.**
- **IV: Device 3rd quadrant conduction, resistive energy dissipation via device, inductor is discharged by the power supply.**

GaN HEMTs withstand surge energy by LC resonance, with minimal resistive energy dissipation in the resonant withstand process

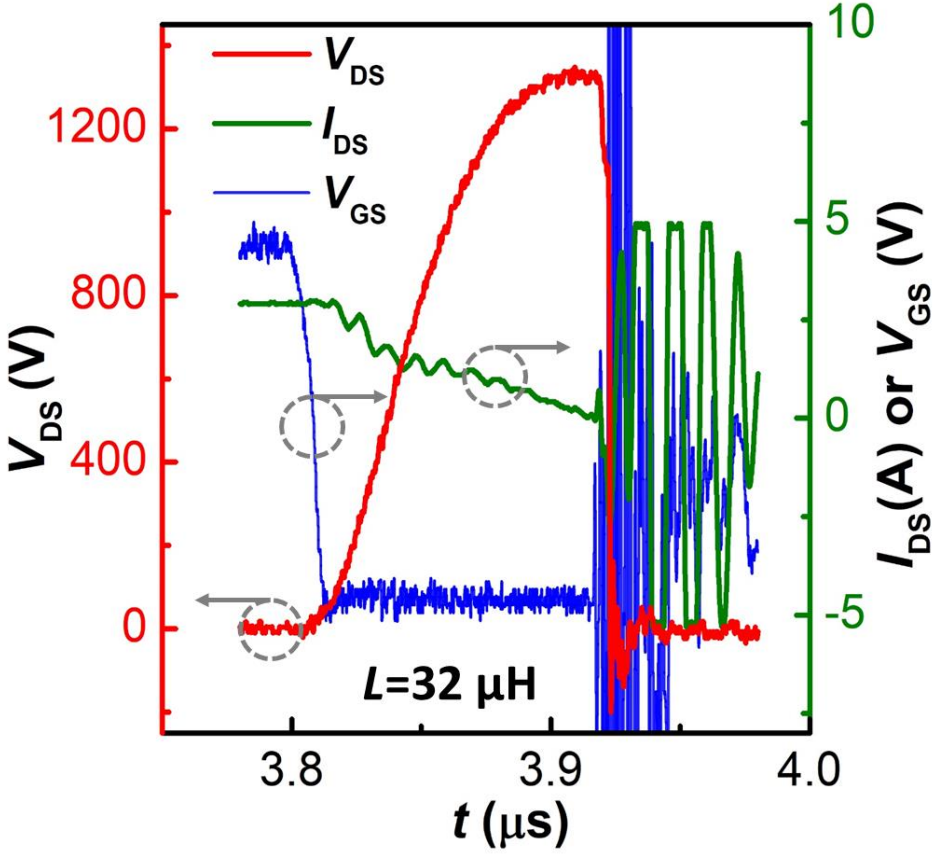
R. Zhang *et al.*, "surge energy and overvoltage ruggedness of p-gate GaN HEMTs", TPEL, early access online, 2020.

UIS Test Result – Failure Waveforms

Company A: GIT



Company B: SP-HEMT



Gate is still functional after the failure

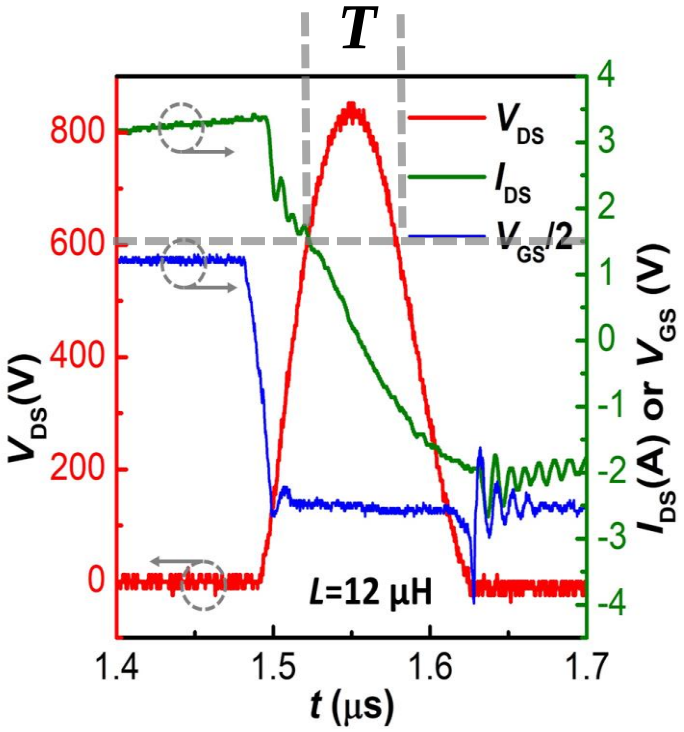
All terminals show short, gate control lost

R. Zhang *et al*., "surge energy and overvoltage ruggedness of p-gate GaN HEMTs", TPEL, early access online, 2020.

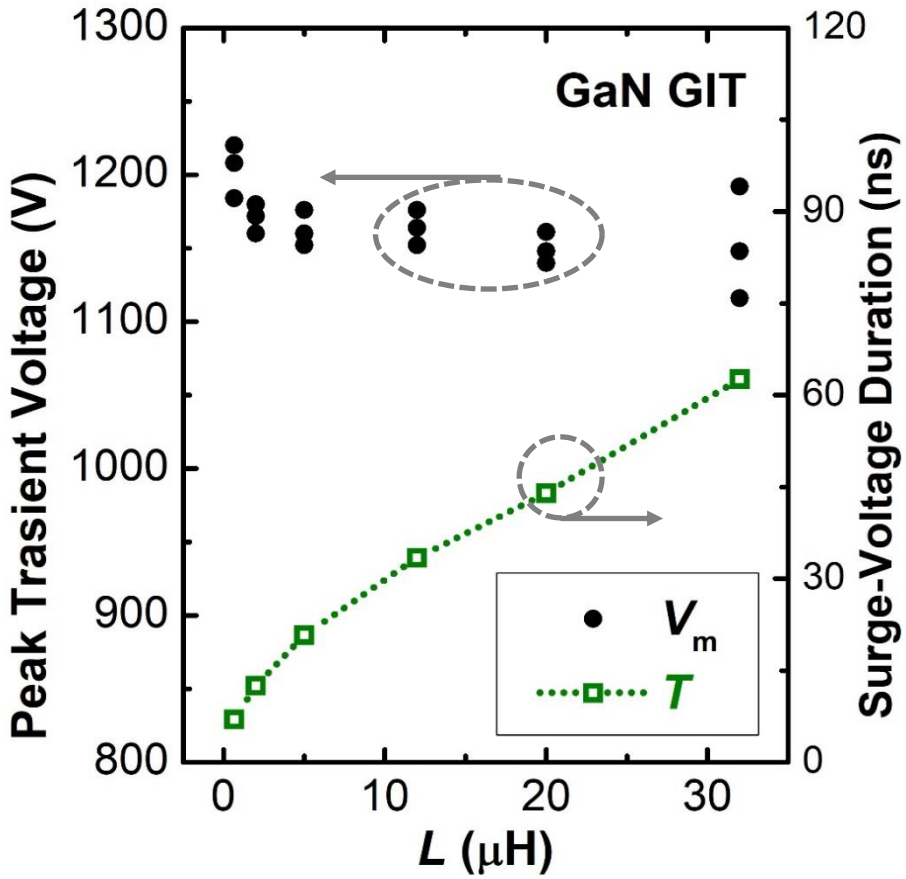
UIS Test Result – Failure Determinist

L: (a) $dV/dt \approx 2V_m/(\pi\sqrt{LC_{oss}})$

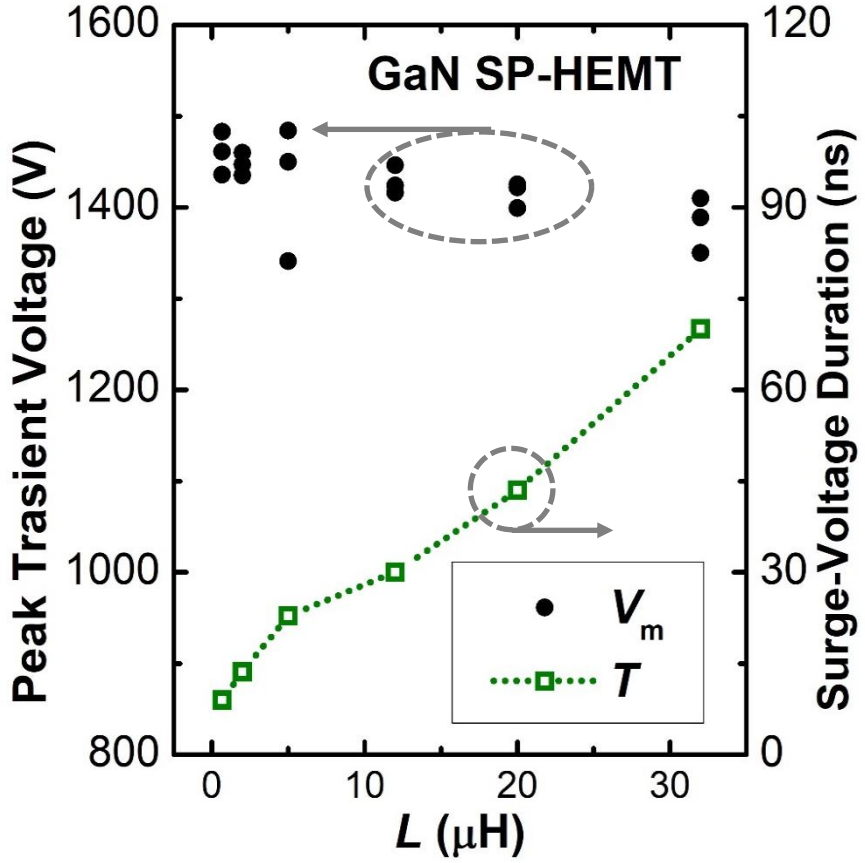
(b) $T: V_{DS} > V_{rating}$



Company A: GIT



Company B: SP-HEMT

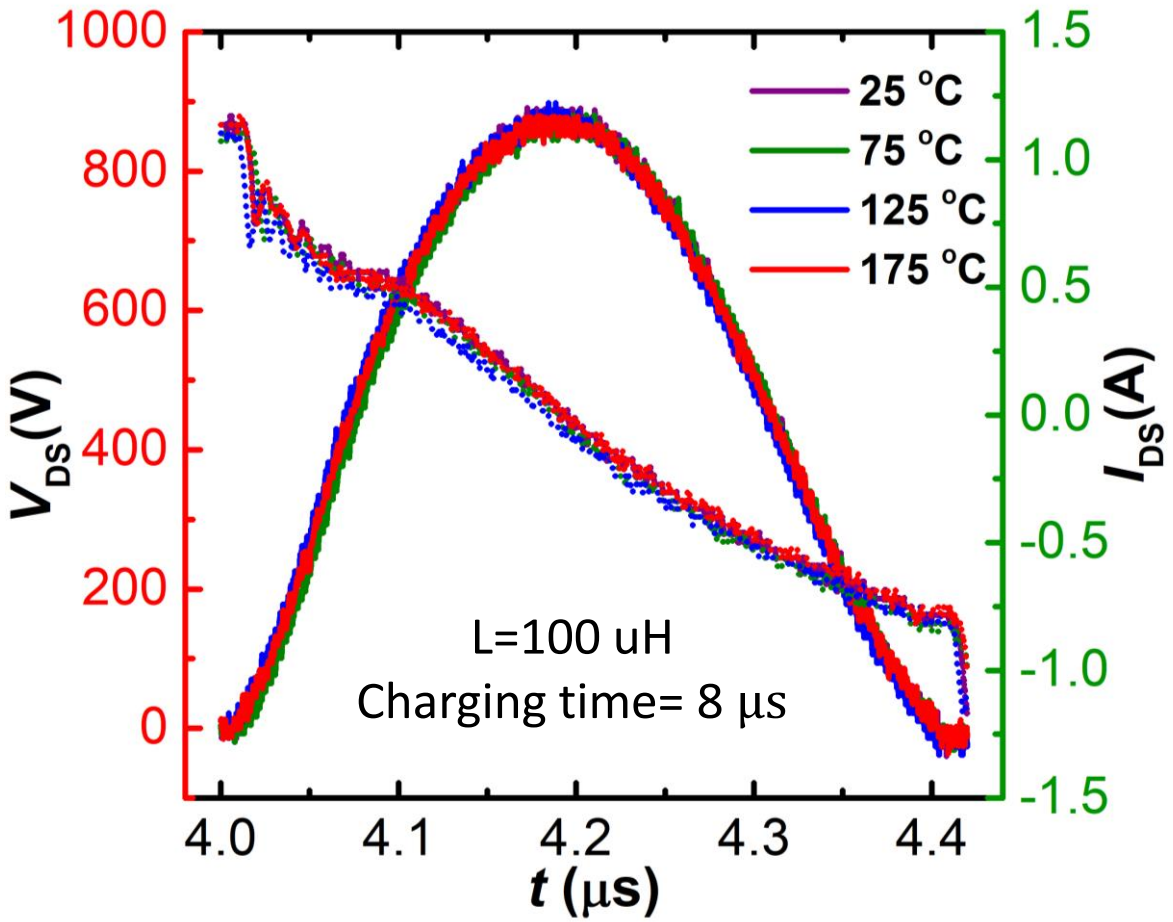


V_m leads to device failure shows little dependence on surge voltage duration within tens of nanoseconds.

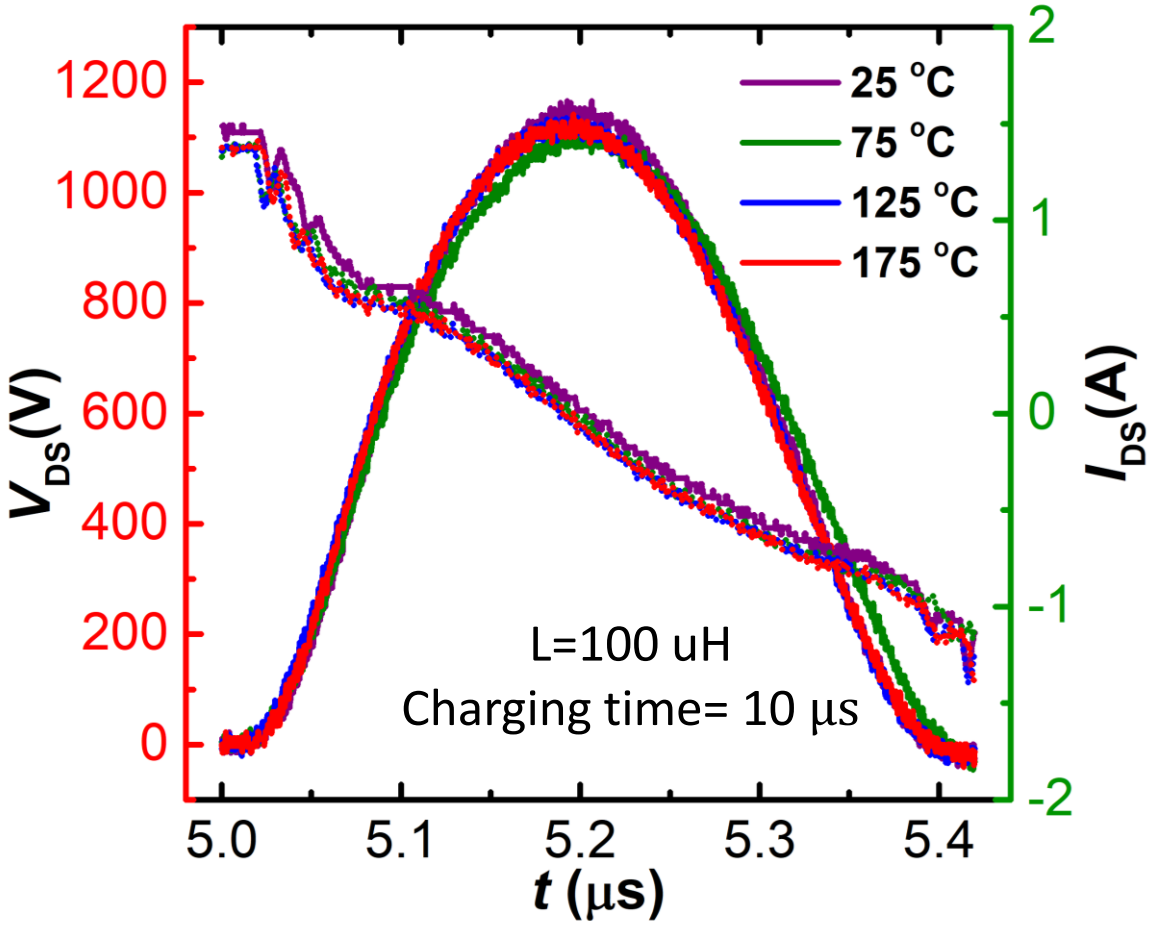
GaN HEMT surge energy capability is almost solely limited by overvoltage capability

High temperature UIS: Safe withstanding waveforms

Company A: GIT



Company B: SP-HEMT

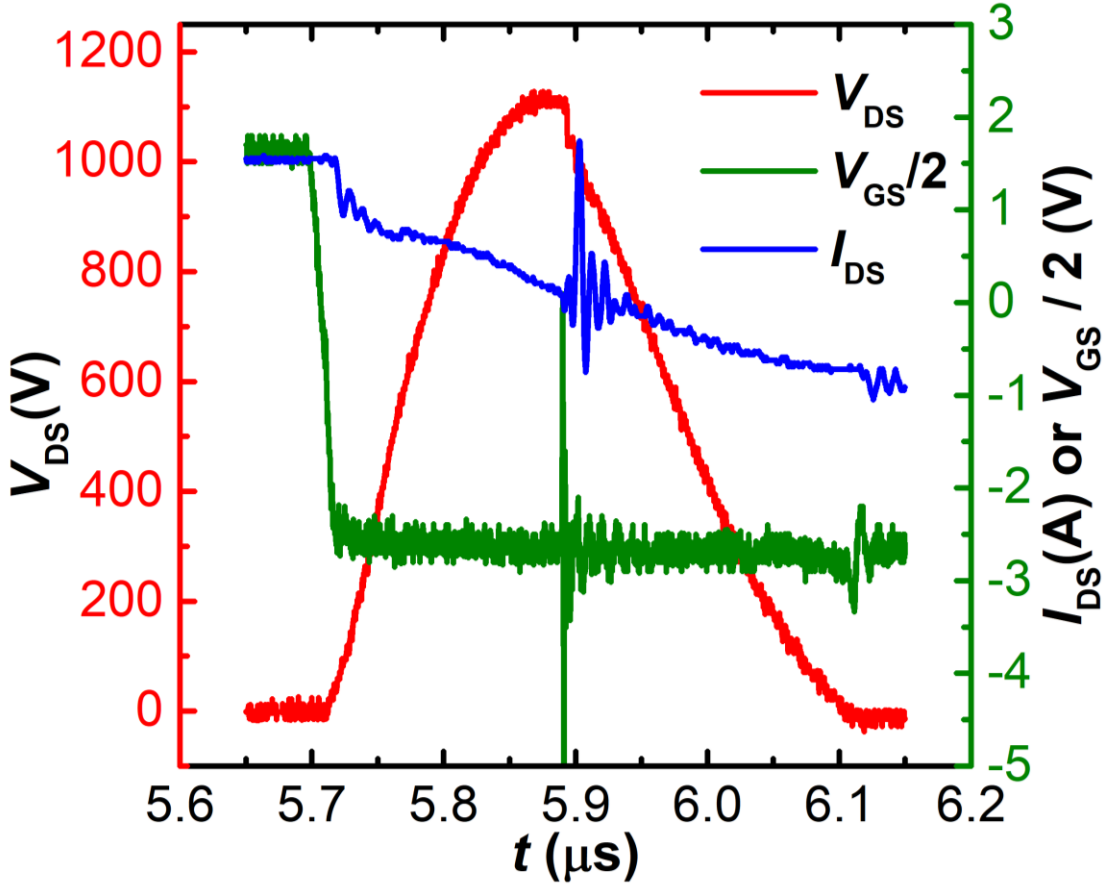


Withstand waveform shows little dependence on temperature

GaN HEMTs C_{oss} changes little with temperature

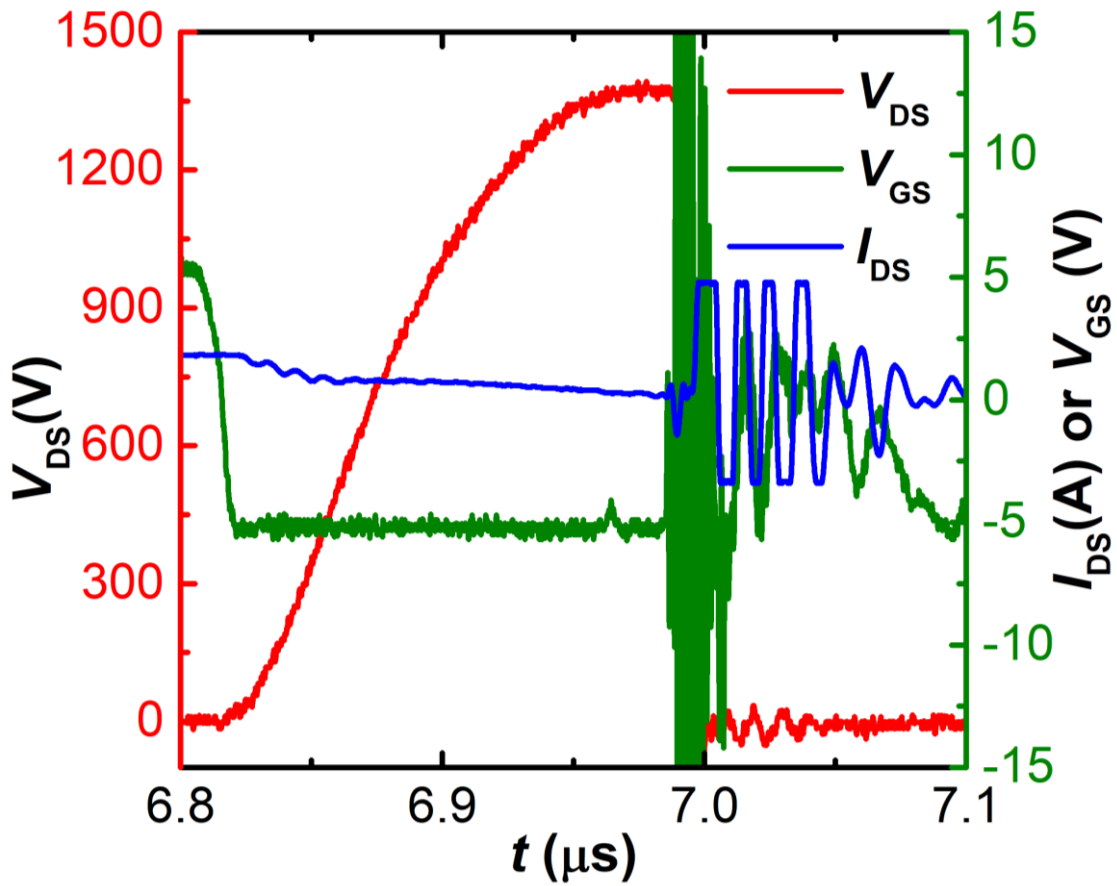
High Temperature (175 °C) UIS: Failure Waveforms

Company A: GIT



T=175 °C
L=100 µH

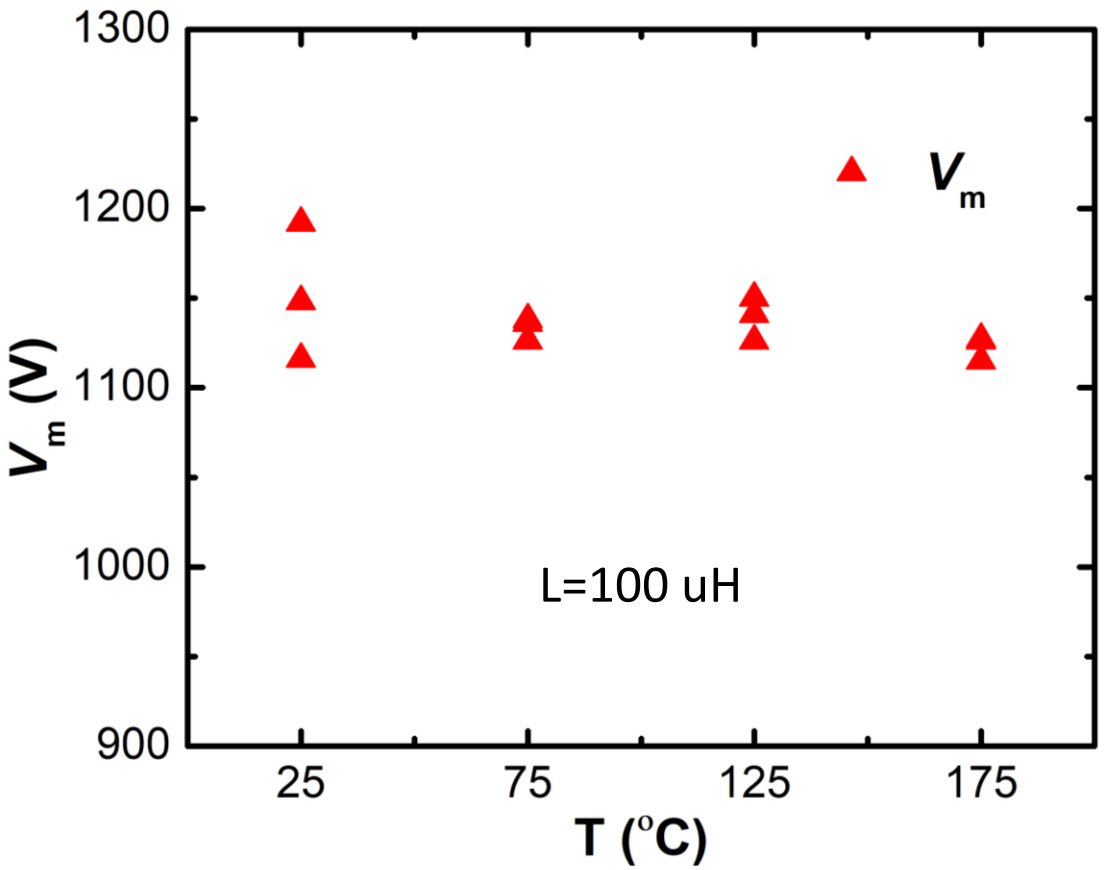
Company B: SP-HEMT



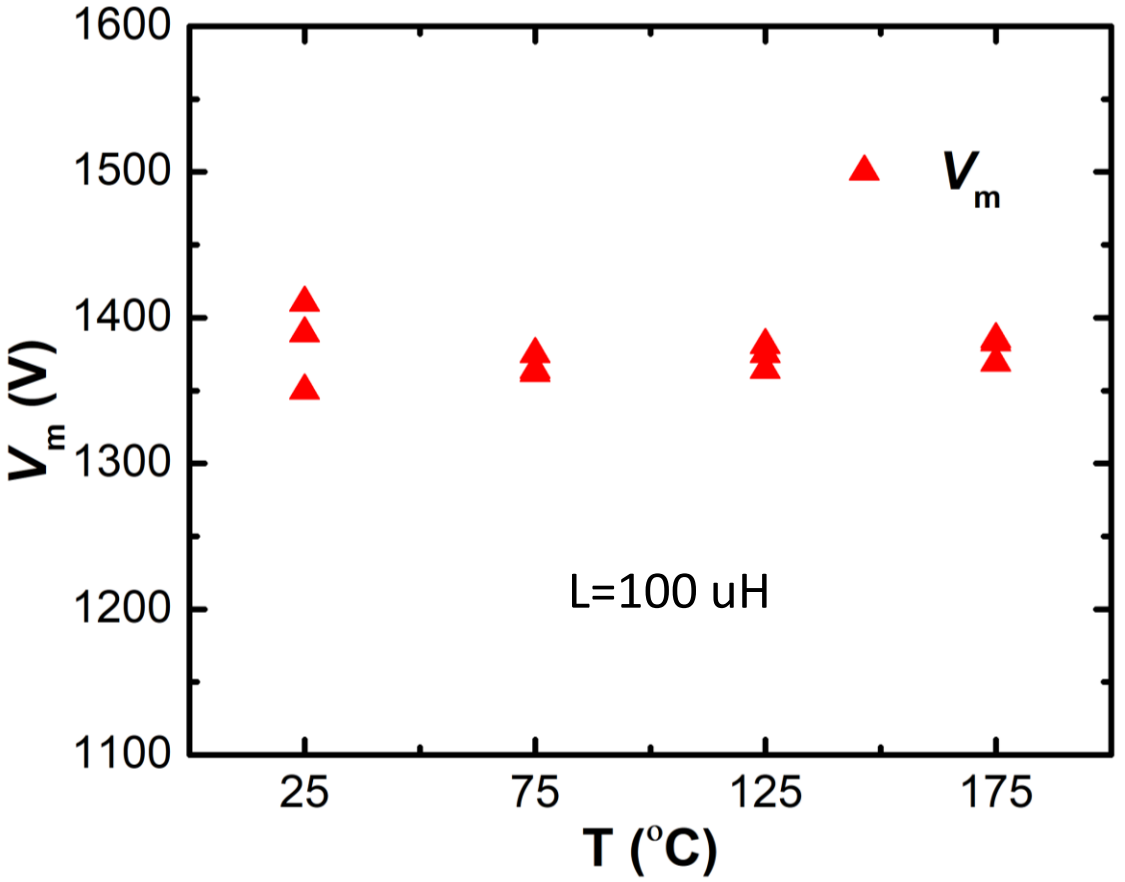
DUTs failed at high temperature show same failure waveforms.
It is believed the failure locations and mechanisms don't change.

High Temperature UIS: Critical V_{DS}

Company A: GIT



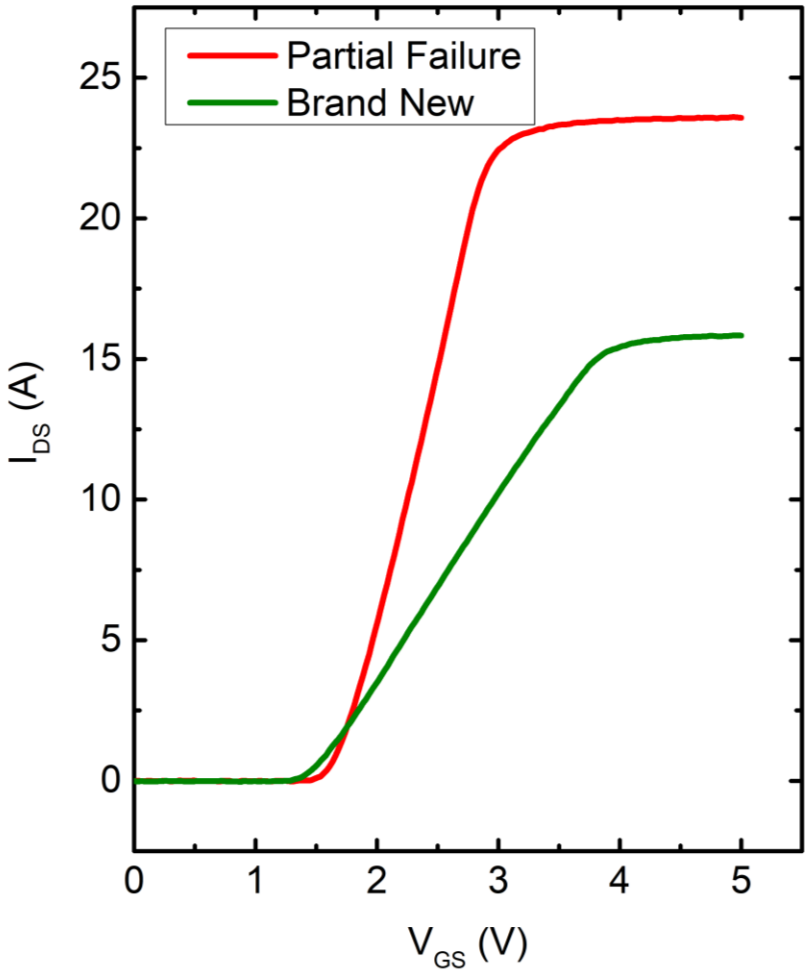
Company B: SP-HEMT



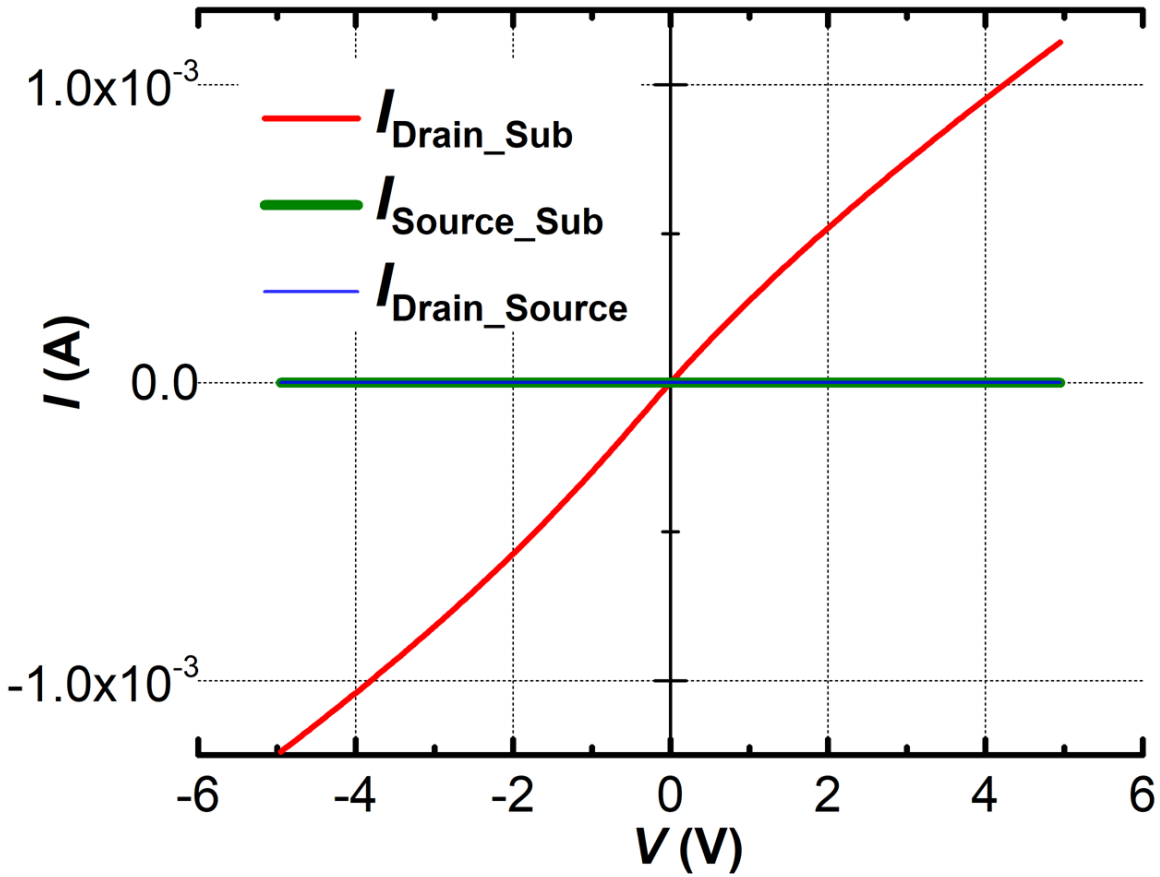
V_m leads to failure see little change in high temperature UIS test.
Failure in UIS test is not related to temperature and is a E-field induced failure

Failure Analysis: GIT – I-V Characterization

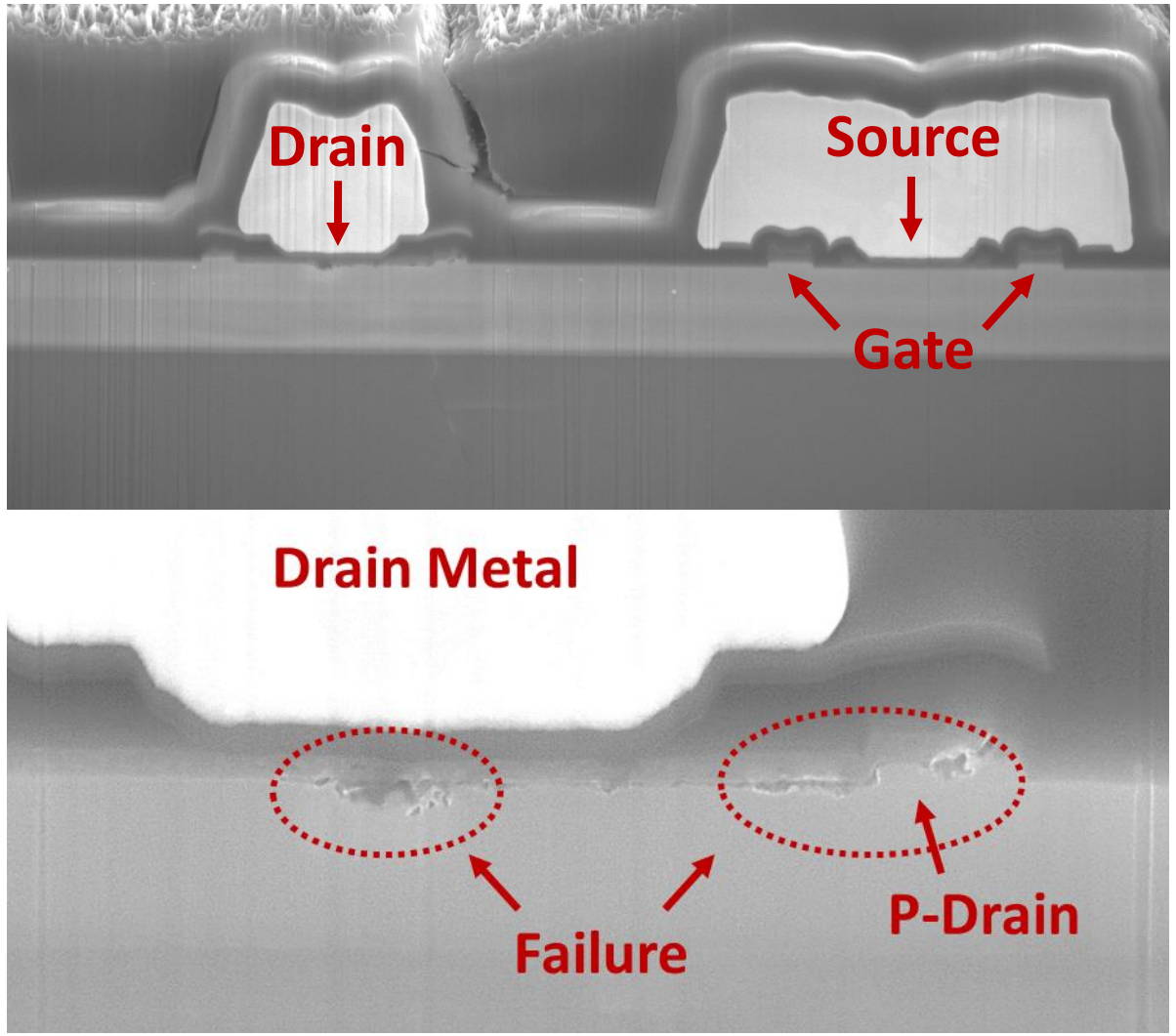
Gate remains functional

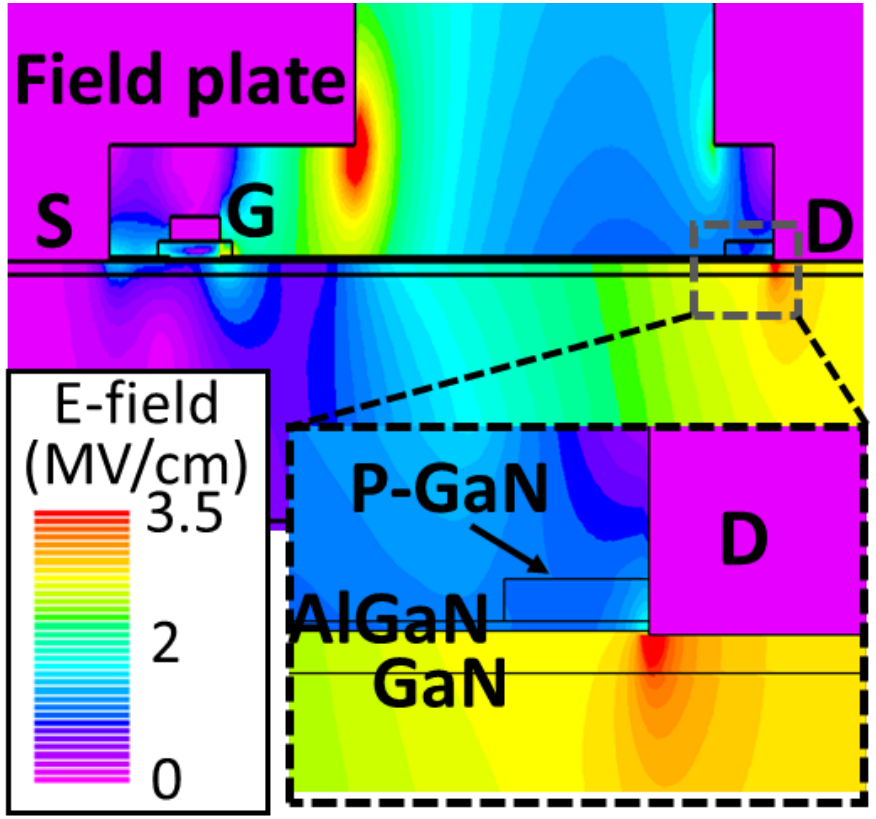


Failure between drain & substrate



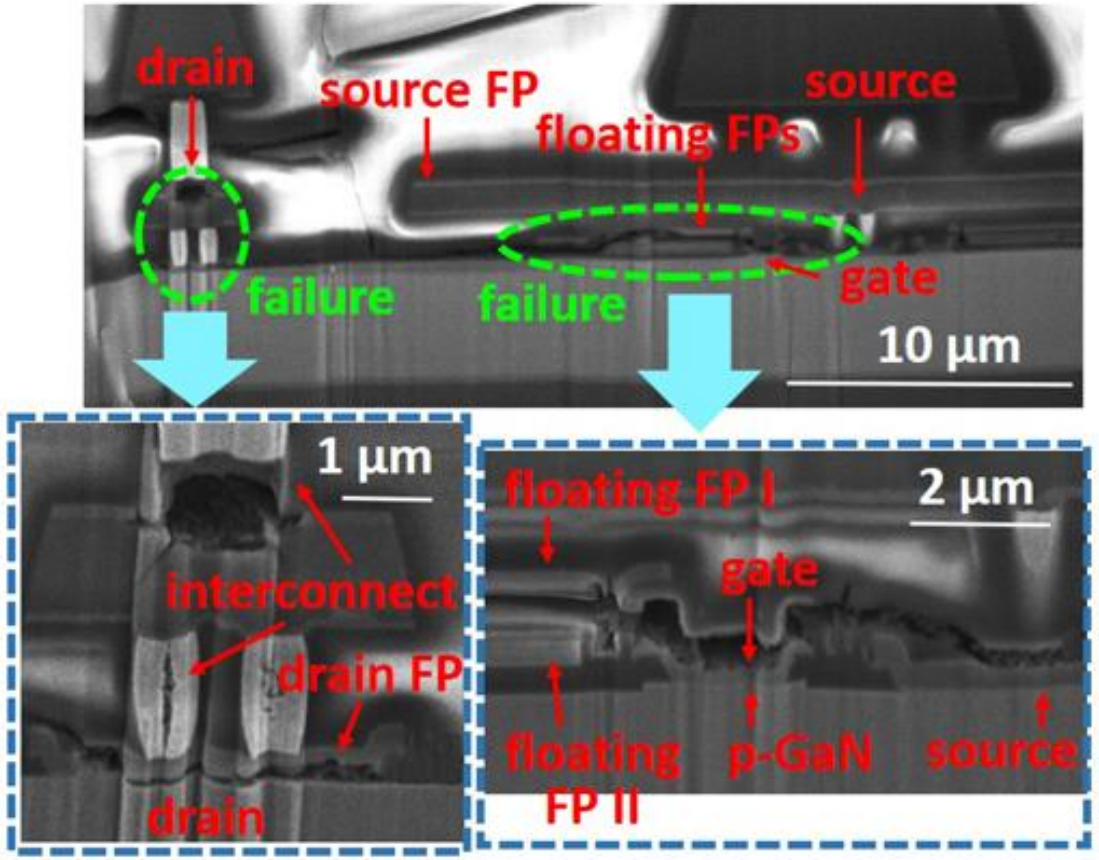
Failure Analysis & Mixed-mode Simulation: GIT

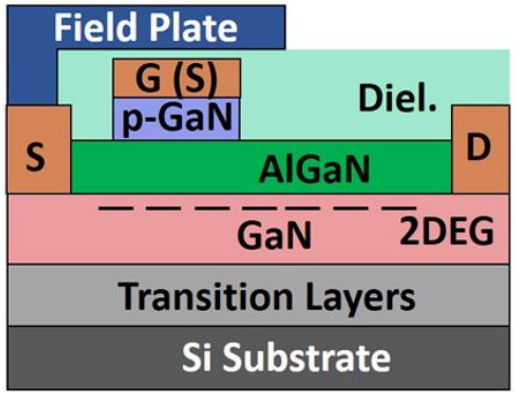


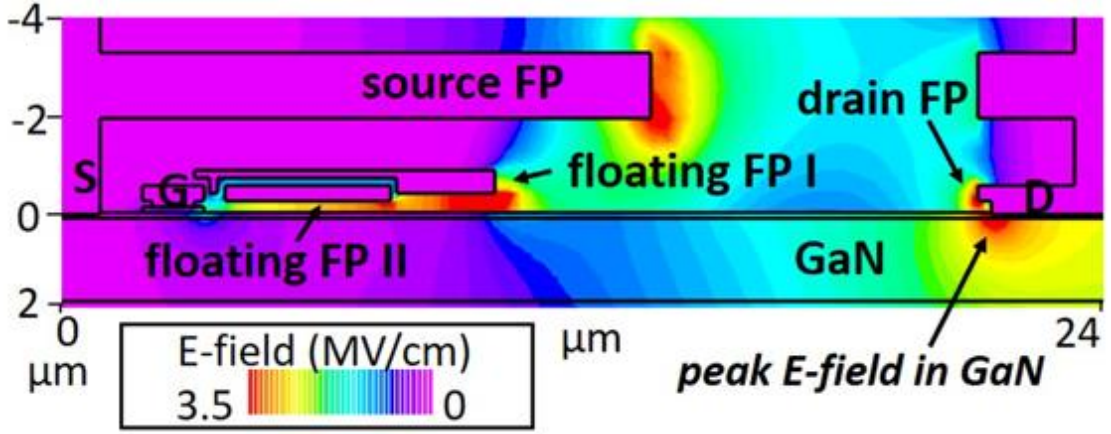


FIB (focused ion-beam) & TCAD simulation: Failure & Peak E-field @ drain

Failure Analysis & Mixed-mode Simulation: SP-HEMT







- Burning (in metal) & cracks (in GaN) found at drain.
- Cracks found at gate field plate but no failure shown in GaN layer in the gate region

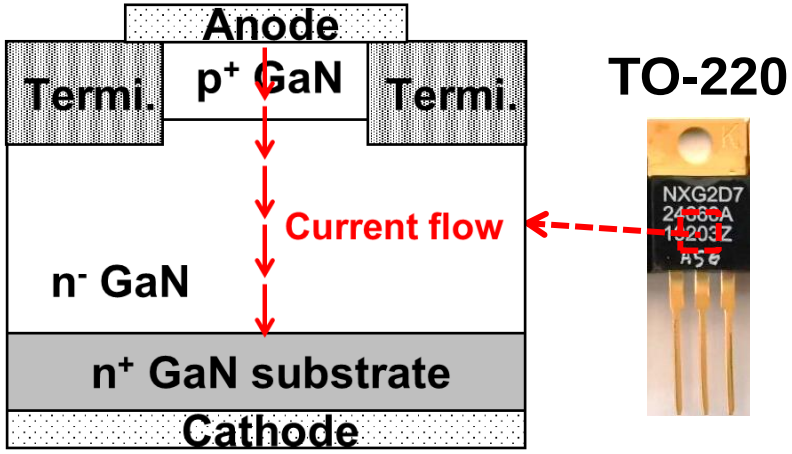
TCAD Simulation: Peak E-field @ drain and floating gate field plate.
Initial failure may locate at drain

Outline

- Introduction
  - Avalanche test: Unclamped Inductive Switching (UIS) test
  - Open question: Avalanche capability in GaN-based power devices
- Avalanche test of 600/650 V lateral HEMTs
  - UIS tests under different temperatures
  - Failure analysis
- Avalanche test of 1200 V vertical GaN PN diode
  - Device static characterization
  - UIS tests under different temperatures
- Summary & Future Work

Devices under Test

- **Vertical GaN PN diode**
- **1.2 kV, > 100 A (pulsed)**



TO-220

Epitaxy growth & device fabrication by NexGen Power Systems in NexGen's 100-mm GaN-on-GaN facility in New York

Properties	GaN-on-Si	GaN-on-GaN
Lattice mismatch (%)	17	0
CTE * mismatch (%)	54	0
Dislocation density (cm^{-2})	10^8-10^9	10^3-10^6
Max. epi-layer thickness (μm)	~5	≥40
Thermal resistance (°C·mm/W) [5]	~30	~4

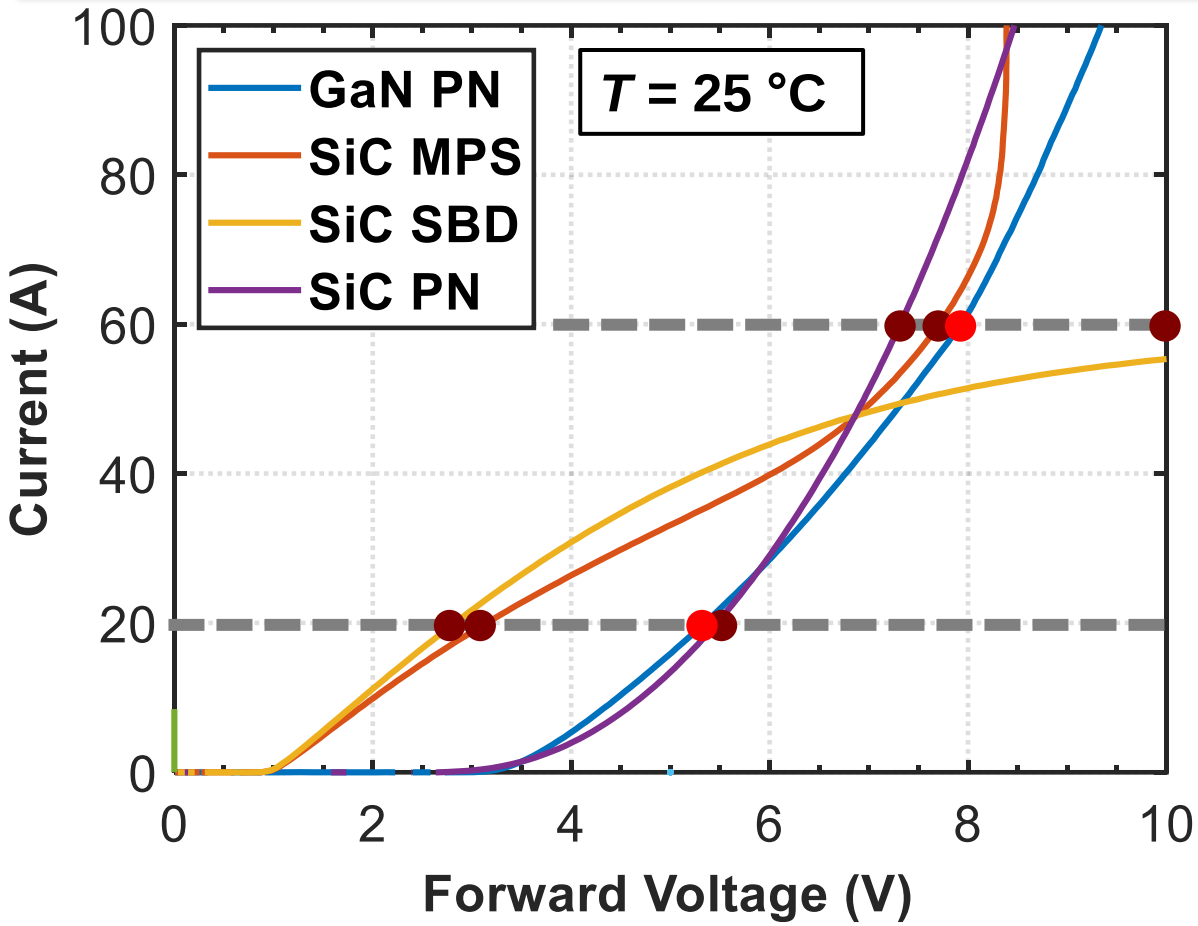
*CTE: Coefficient of thermal expansion.

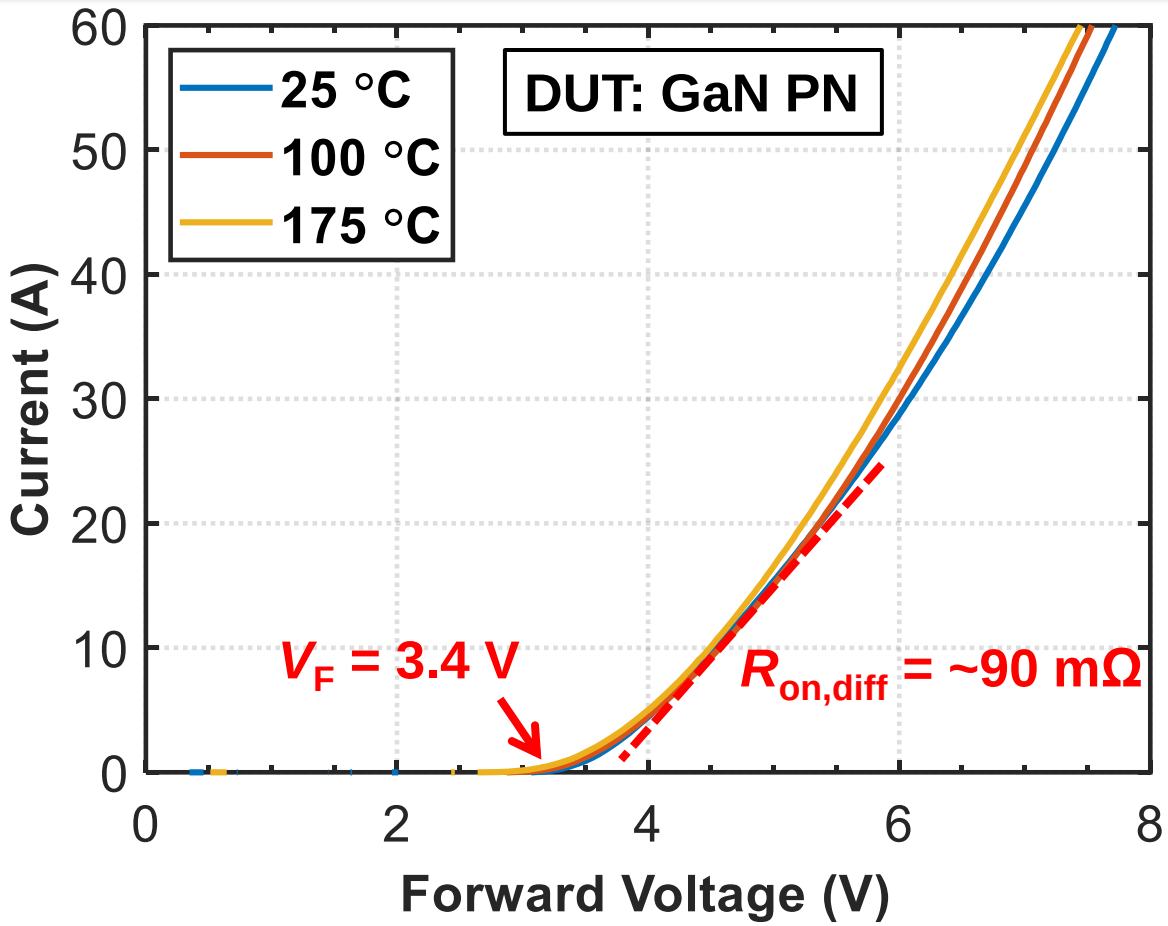
Source: *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5012–5018, 2019.

- **Compare with commercial 1.2 kV SiC Devices:**
  - Merged PN Schottky (MPS) diode
  - Schottky barrier diode (SBD)
  - PN diode (i.e. body diode of MOSFET)

Device Tech.	Vendor	Part #	Nominal Current	Current @25 °C	Package
MPS	Infineon	IDH05G120C5	5 A @161 °C	19.1 A	TO-220
SBD	Rohm	SCS205KG	5 A @150 °C	-	TO-220
PN	Cree	C2M0160120D	-	25 A	TO-247

Characterization: Forward I-V





- Loss @ nominal current level (20 A):

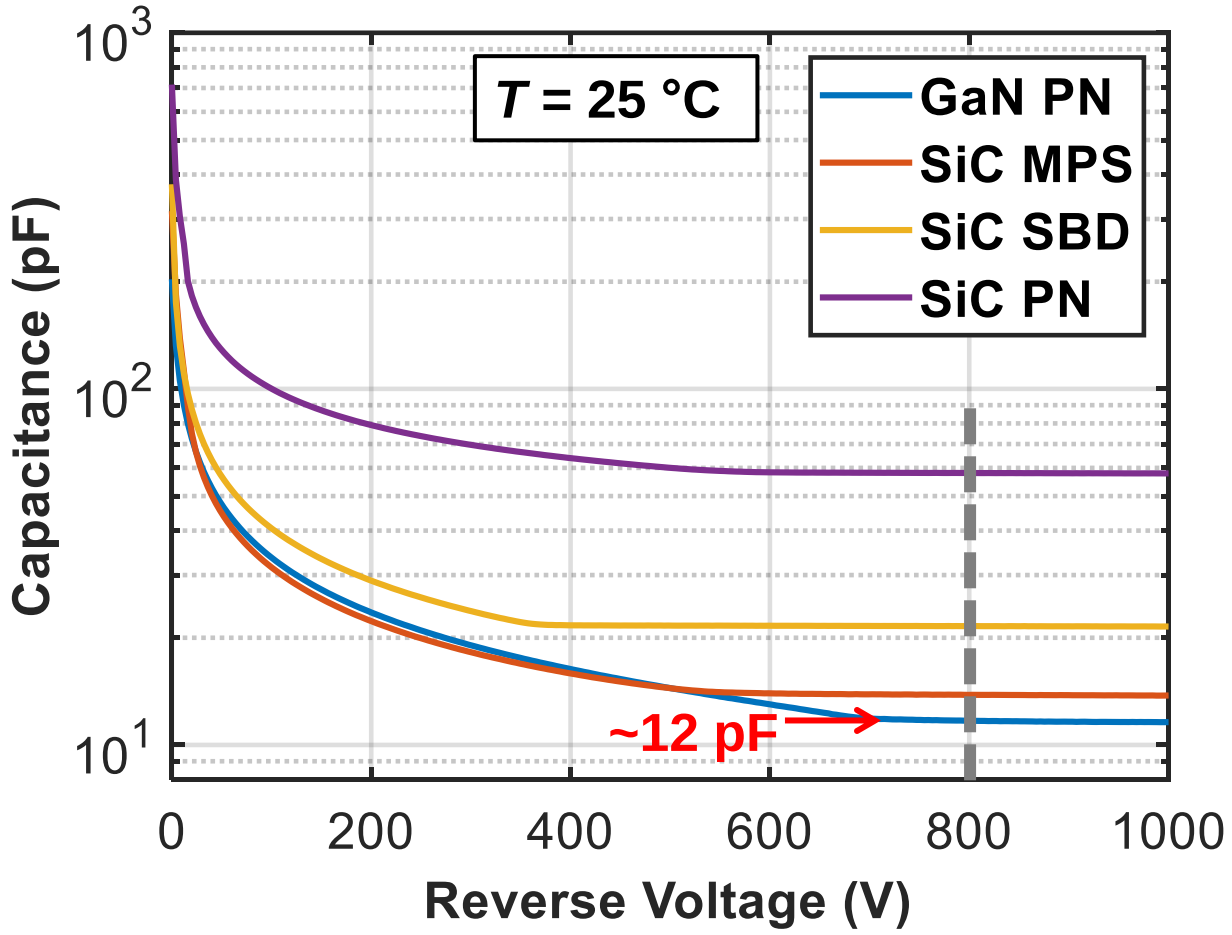
SiC SBD < SiC MPS < GaN PN ≈ SiC PN

- Loss @ surge current level (60 A):

GaN PN close to SiC PN & MPS, << SiC SBD

- Forward characteristics of GaN PN varies little with temperature

Characterization: C-V



DUT	Total charge (nC) (V_R = 800 V)
GaN PN	17.82
SiC MPS	18.40
SiC SBD	24.28
SiC PN	62.99

$$Q_C = \int_0^{V_R} C(V)dV$$

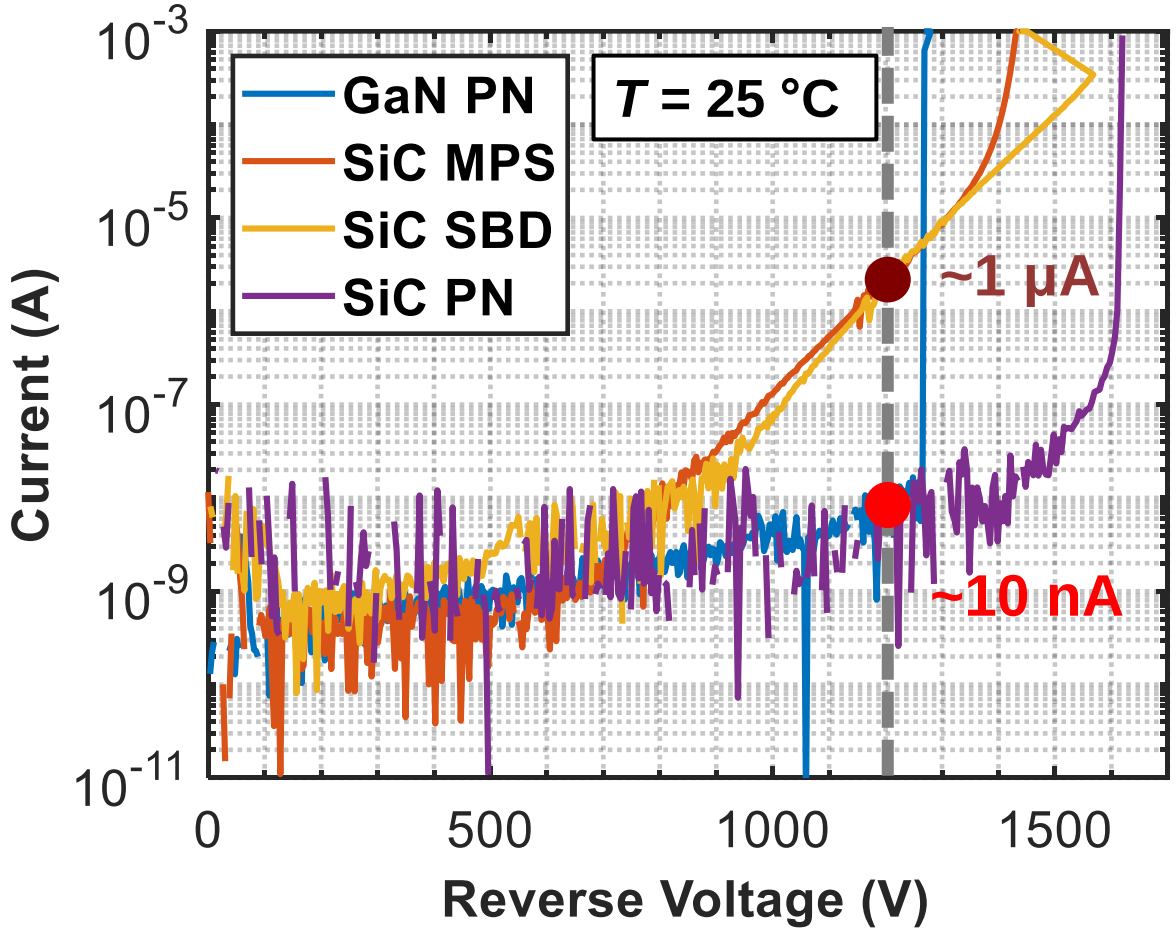
DUT	Capacitance stored energy(μJ) (V_R = 800 V)
GaN PN	4.89
SiC MPS	5.07
SiC SBD	7.36
SiC PN	20.21

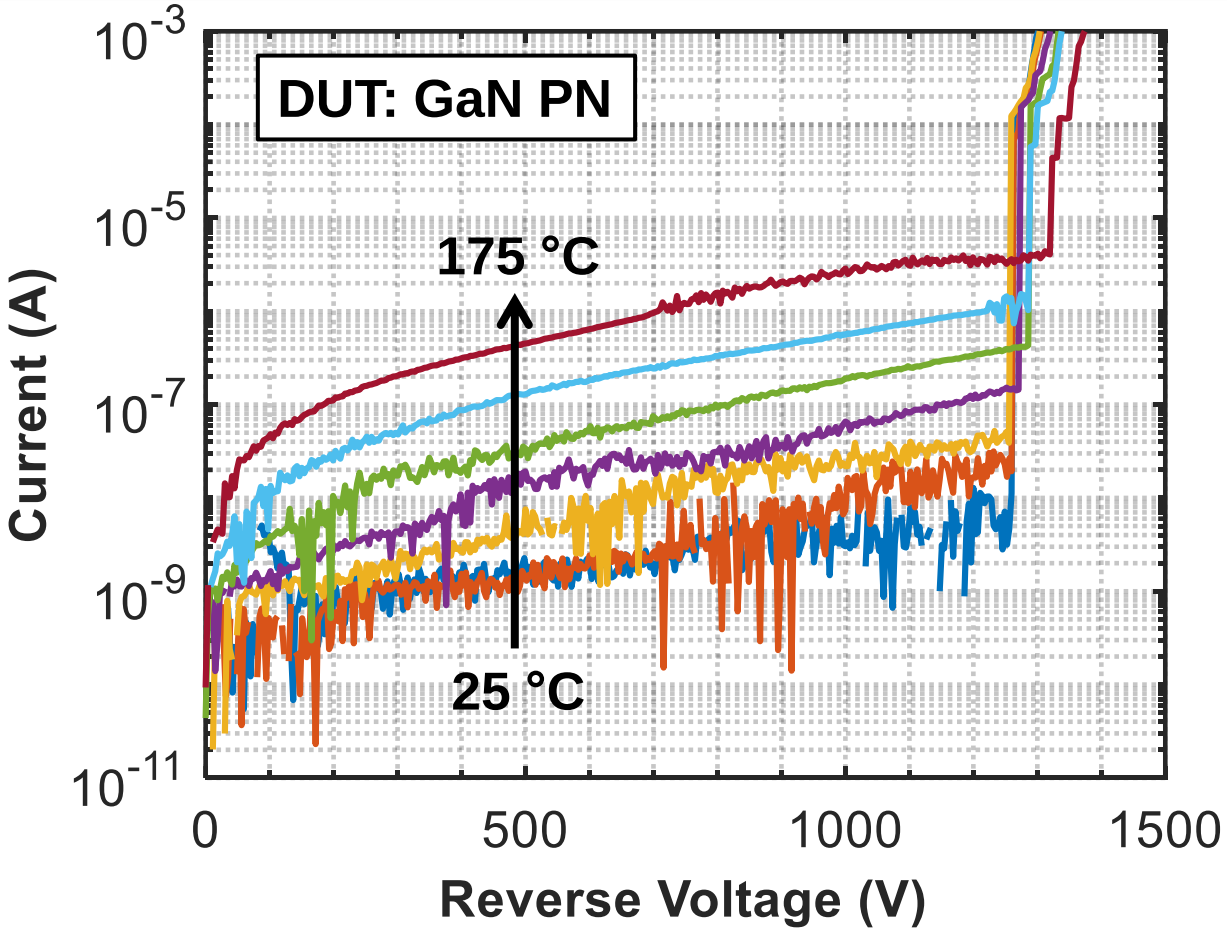
$$E_C = \int_0^{V_R} C(V)VdV$$

- No reverse recovery
- C & Q_C & E_C:

GaN PN < SiC MPS < SiC SBD < SiC PN

Characterization: Reverse I-V





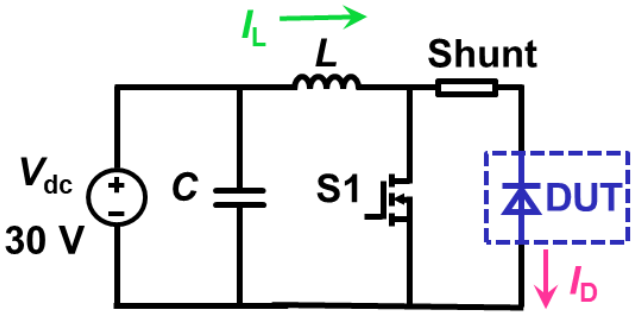
- Breakdown voltage > 1200 V
- Leakage current @ 1200 V:

GaN PN ≈ SiC PN < SiC MPS ≈ SiC SBD

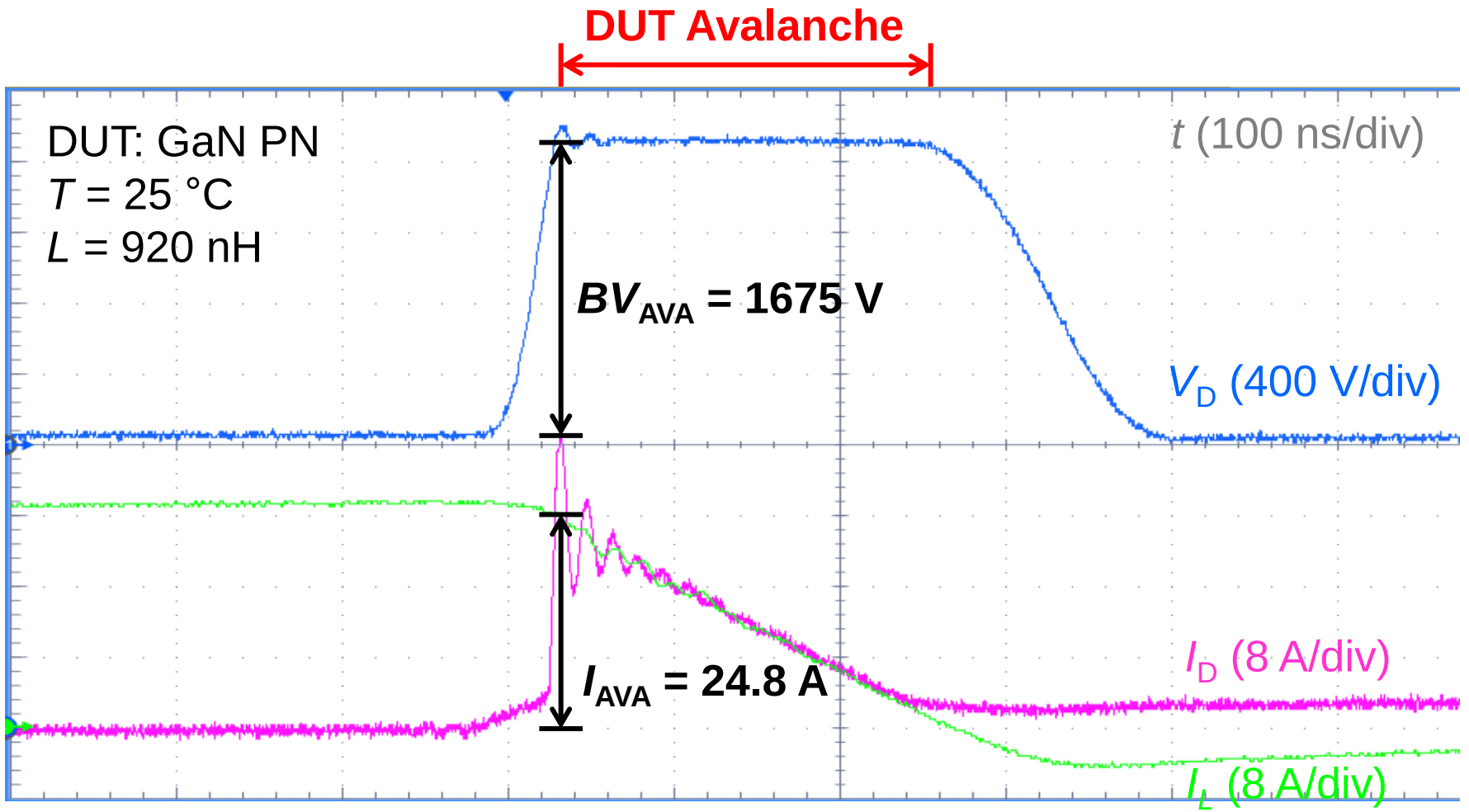
- Leakage increases with temperature
- BV increases with temperature
  -> Avalanche nature

UIS Test

- **Unclamped inductive switching (UIS) circuit**
  - S1 = 1.7 kV SiC MOSFET



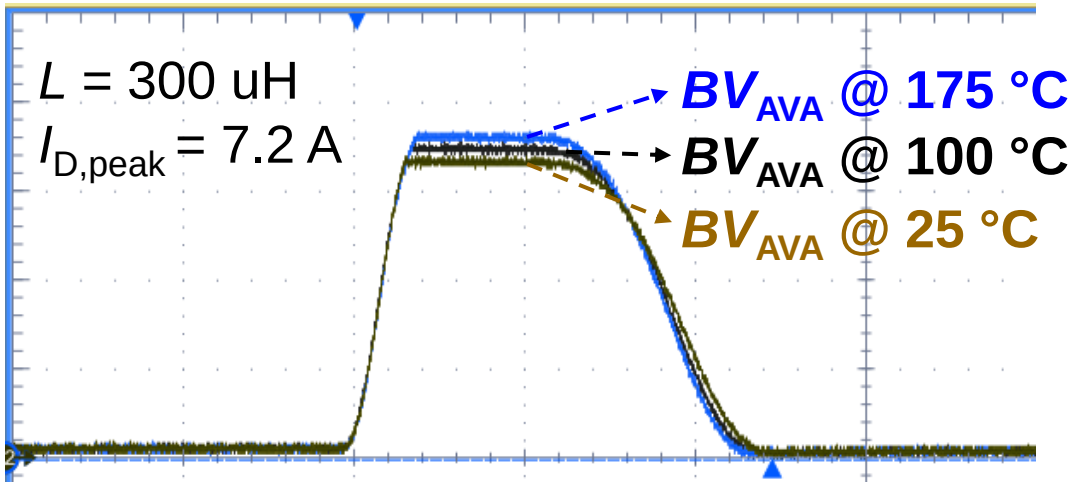
- **Test condition**
  - **6 inductors:** 920 nH to 81 mH
  - **3 temperatures:** 25 °C, 100 °C, 175 °C

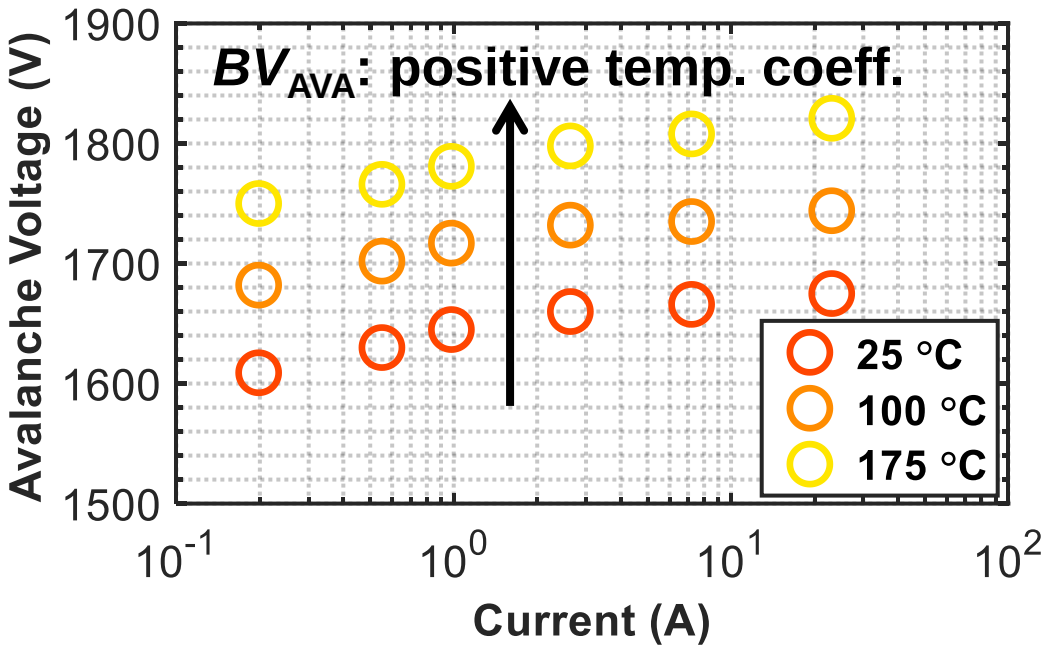


➢ **Robust avalanche demonstrated**

UIS test

- **Robust avalanche capability under elevated temperatures**



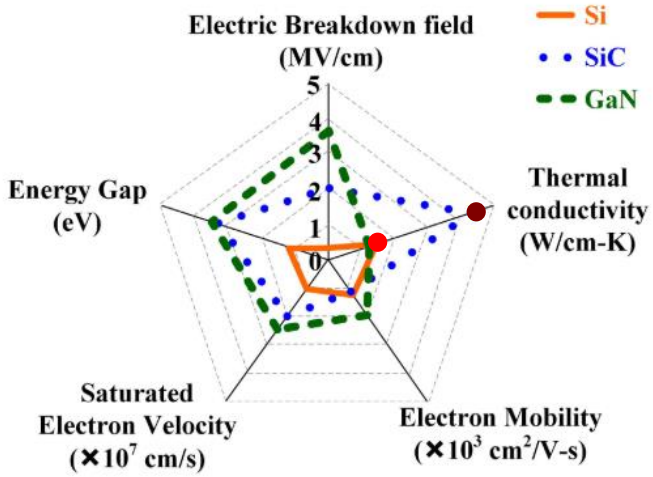


- **Failure mode: Thermally induced destruction**

- Critical E_{AVA} roughly consistent with thermal conductivity:

GaN (1.3 ~ 2) < 4H-SiC (3.7)

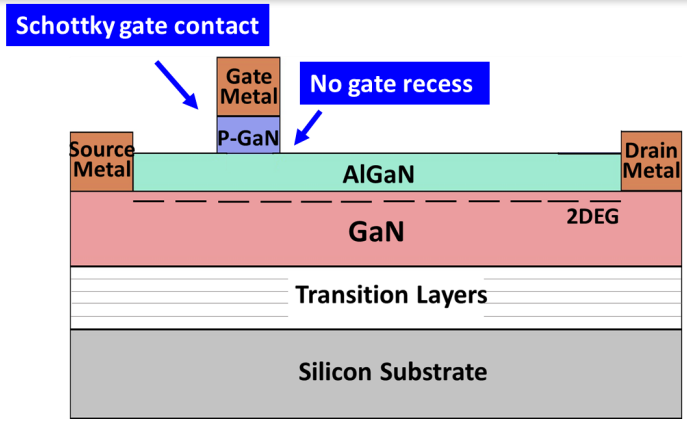
DUT	Critical Ava. Energy (J/cm²)
GaN PN	2.6
SiC MPS	5.0
SiC SBD	2.0
SiC PN	6.7

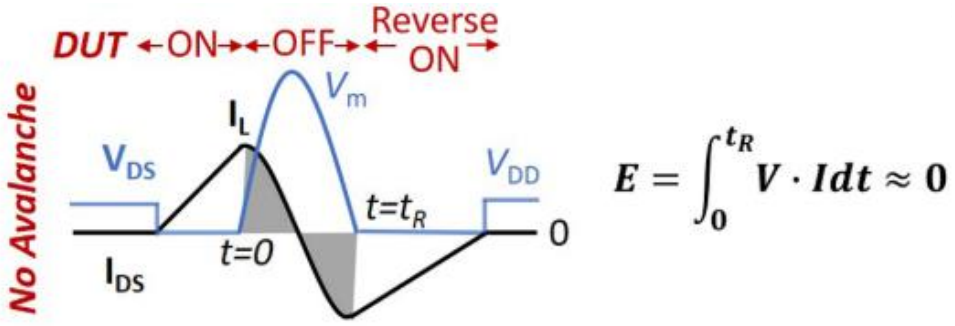


Outline

- Introduction
  - Avalanche test: Unclamped Inductive Switching (UIS) test
  - Open question: Avalanche capability in GaN-based power devices
- Avalanche test of 600/650 V lateral HEMTs
  - UIS tests under different temperatures
  - Failure analysis
- Avalanche test of 1200 V vertical GaN PN diode
  - Device static characterization
  - UIS tests under different temperatures
- Summary & Future Work

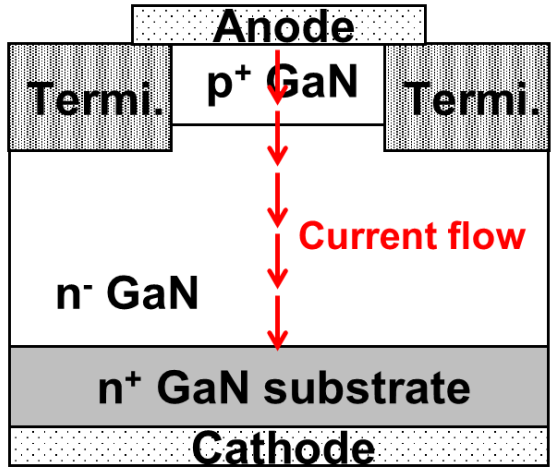
Summary – Avalanche Ruggedness of GaN Devices

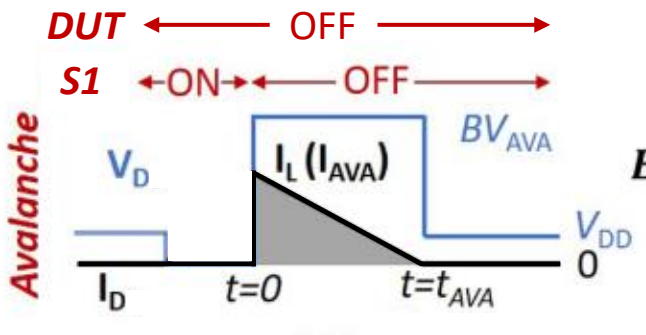




$$E = \int_0^{t_R} V \cdot Idt \approx 0$$

- GaN HEMTs "avalanche capability" limited by transient breakdown voltage, the failure is induced by high E-field.
- Different failure locations were found in commercial GITs and SP-HEMTs
- Failure mechanisms, boundaries, and failure locations are not influenced by temperature.

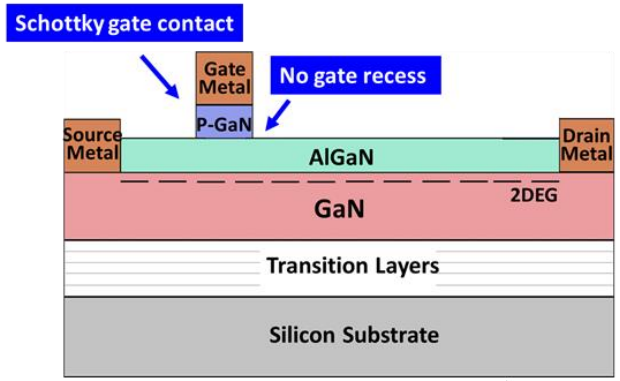


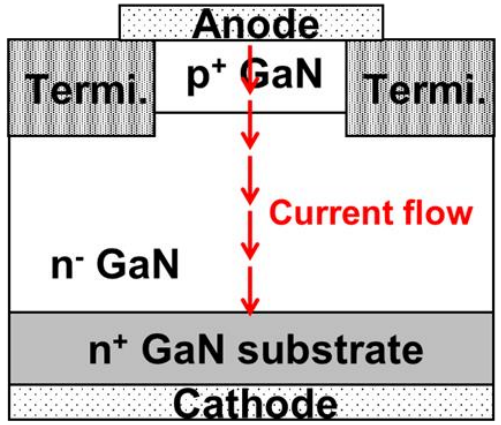


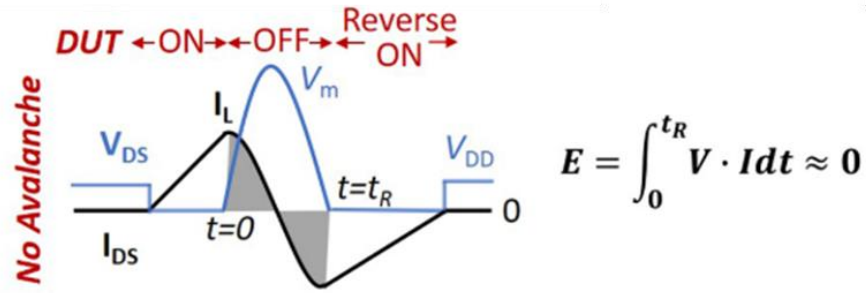
$$E_{AVA} = \int_0^{t_{AVA}} V \cdot Idt = \frac{LI_{AVA}^2 BV_{AVA}}{2(BV_{AVA} - V_{DD})}$$

- Large-area 1.2 kV vertical GaN PN diodes with current up to 100 A, manufactured by NexGen
- Vertical GaN-on-GaN PN diode demonstrated robust avalanche
- Failure mode: thermally induced
- GaN can avalanche!

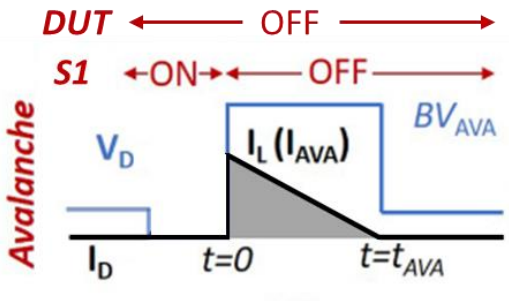
Next Steps







$$E = \int_0^{t_R} V \cdot Idt \approx 0$$



$$E_{AVA} = \int_0^{t_{AVA}} V \cdot Idt = \frac{LI_{AVA}^2 BV_{AVA}}{2(BV_{AVA} - V_{DD})}$$

- **Repetitive UIS tests for lateral GaN HEMTs and vertical GaN PN diodes.**
- **Design and develop GaN HEMT surge ruggedness under converter mission profiles.**
- **Surge ruggedness of GaN transistors.**

Thank you!

Contacts: Ruizhe Zhang (rzzhang@vt.edu), Jingcun Liu (jcliu@vt.edu), Yuhao Zhang (yhzhang@vt.edu)